Memory and Channel Specifications

Controller/ Cat. No.	Maximum User Memory Words	Total I/O Maximum (Any Mix)	Types of Communication Ports	Maximum Number of I/O Racks (Rack Addresses)	Maximum Number of I/O Chassis		
					Total	Ext Local	Remote
PLC-5/11 (1785-L11B)	8 K	512 (any mix) or 384 in + 384 out (complementary)	1 DH+/Remote I/O (Adapter or Scanner) 1 serial port, configurable for RS-232 and 423 and RS-422A compatible	4 (0-3)	5	0	4 (must be rack 3)
PLC-5/20 (1785-L20B) PLC-5/26 (1785-L26B)	16K	512 (any mix) or 512 in + 512 out (complementary)	1 DH+ (Fixed) 1 DH+/Remote I/O (Adapter or Scanner) 1 serial port, configurable for RS-232 and 423 and RS-422A compatible	4 (0-3)	13	0	12
PLC-5/20E (1785-L20E)	16K	512 (any mix) or 512 in + 512 out (complementary)	1 DH+ (Fixed) 1 DH+/Remote I/O (Adapter or Scanner) 1 serial port, configurable for RS-232 and 423 and RS-422A compatible 1 channel Ethernet only	4 (0-3)	13	0	12
PLC-5/30 (1785-L30B)	32 K	1024 (any mix) or 1024 in and 1024 out (complementary)	2 DH+/Remote I/O (Adapter or Scanner) 1 serial port, configurable for RS-232 and 423 and RS-422A compatible	8 (0-7)	29	0	28
PLC-5/40 (1785-L40B) PLC-5/46 (1785-L46B)	48 K(1)	2048 (any mix) or 2048 in + 2048 out (complementary)	4 DH+/Remote I/O (Adapter or Scanner) 1 serial port, configurable for RS-232 and 423 and RS-422A compatible	16 (0-17)	61	0	60
PLC-5/40E (1785-L40E)	48 K1	2048 (any mix) or 2048 in + 2048 out (complementary)	2 DH+/Remote I/O (Adapter or Scanner) 1 channel Ethernet only 1 serial port, configurable for RS-232 and 423 and RS-422A compatible	16 (0-17)	61	0	60
PLC-5/40L (1785-L40L)	48 K1	2048 (any mix) or 2048 in + 2048 out (complementary)	2 DH+/Remote I/O (Adapter or Scanner) 1 serial port, configurable for RS-232 and 423 and RS-422A compatible 1 Extended-Local I/O	16 (0-17)	61	16	60

Controller/ Cat. No.	Maximum User Memory Words	Total I/O Maximum (Any Mix)	Types of Communication Ports	Maximum Number of I/O Racks (Rack Addresses)	Maximum Number of I/O Chassis		
PLC-5/60 (1785-L60B)	64 K(2)	3072 (any mix) or 3072 in + 3072 out (complementary)	4 DH+/Remote I/O (Adapter or Scanner) 1 serial port, configurable for RS-232 and 423 and RS-422A compatible	24 (0-27)	93	0	92
PLC-5/60L (1785-L60L)	64 K[2]	3072 (any mix) or 3072 in + 3072 out (complementary)	2 DH+/Remote I/O (Adapter or Scanner) 1 serial port, configurable for RS-232 and 423 and RS-422A compatible 1 Extended Local I/O	24 (0-27)	81	16	64
PLC-5/80 (1785-L80B) PLC-5/86 (1785-L86B)	100 K(3)	3072 (any mix) or 3072 in + 3072 out (complementary)	4 DH+/Remote I/O (Adapter or Scanner) 1 serial port, configurable for RS-232 and 423 and RS-422A compatible	24 (0-27)	93	0	92
PLC-5/80E (1785-L80E)	100 K[3]	3072 (any mix) or 3072 in + 3072 out (complementary)	2 DH+/Remote I/O (Adapter or Scanner) 1 serial port, configurable for RS-232 and 423 and RS-422A compatible 1 channel Ethernet only	24 (0-27)	65	0	64

[1] The PLC-5/40, -5/40E, -5/40L controllers have a limit of 32K words per data table file.

[2] The PLC-5/60 and -5/60L controllers have a limit of 56K words per program file and 32K words per data table file.

[3] The PLC-5/80, -5/80E controllers have 64K words of total data table space with a limit of 56K words per program file and 32K words per data table file.

Battery Specifications

Enhanced and Ethernet PLC-5 programmable controllers use 1770-XYC batteries that contain 0.65 grams of lithium.

In these Controllers	At this Temperature	Battery Life Estimates		
		Power Off 100%	Power Off 50%	Battery Duration Aafter the LED Lights[1]
PLC-5/11B, -5/20B and -5/20E	60°C	256 days	1.4 years	11.5 days
	25°C	2 years	4 years	47 days
PLC-5/30B -5/40B, -5/40E, -5/40L, -5/60B, -5/60L, -5/80B and -5/80E	60°C	84 days	150 days	5 days
	25°C	1 year	1.2 years	30 days

[1] The battery indicator (BATT) warns you when the battery is low. These durations are based on the battery supplying the only power to the controller (power to the chassis is off) once the LED first lights.

Memory Backup Devices

You can add an EEPROM to the PLC-5 controller to provide backup memory for your program in case the controller loses power. These memory cards are available:

Catalog Number	For This Product	Memory Size
1785-ME16	Enhanced PLC-5 controllers	16K words
1785-ME32	Enhanced PLC-5 controllers	32K words
1785-ME64	Enhanced PLC-5 controllers	64K words
1785-ME100	Enhanced PLC-5 controllers	100K words

Use your programming software to save a program currently in the controller to the EEPROM card. If you restore a program from the EEPROM to controller memory and controller memory is bad, the restore changes the date and time in the controller status file to the date and time the EEPROM was saved. If you restore a program from the EEPROM to controller memory and controller memory is valid, the status file retains its current date and time.

EEPROM Compatibility

EEPROM compatibility is related to:

Area	Description
ControlNet PLC-5 controllers	EEPROM memory cannot be loaded to a non-ControlNet PLC-5 controller if the EEPROM was saved on a ControlNet PLC-5 controller. EEPROM memory cannot be loaded to a ControlNet PLC-5 controller if the EEPROM was burned on a non-ControlNet PLC-5 controller.
PLC-5 catalog numbers	EEPROM memory can be loaded to a PLC-5 controller if its I/O memory size is greater than or equal to the I/O memory of the PLC-5 controller from which the EEPROM was saved. The I/O memory sizes are: PLC-5/11, -5/204 racks PLC-5/308 racks PLC-5/4016 racks PLC-5/60, -5/8024 racks EEPROM memory can be loaded to a PLC-5 controller if its user memory is greater than or equal to the user memory used on the PLC-5 controller from which the EEPROM was saved. The available user memory is: PLC-5/118,192 words PLC-5/2016,384 words PLC-5/3032,768 words PLC-5/4065,536 words PLC-5/80102,400 words
Firmware release compatibility	EEPROM memory saved on a series D, revision B PLC-5 controller cannot be loaded on a PLC-5 controller with an earlier firmware release. EEPROM memory saved on a series E, revision A PLC-5 controller cannot be loaded on a PLC-5 controller with an earlier firmware release. EEPROM memory saved on a series E, revision B PLC-5 controller cannot be loaded on a PLC-5 controller with an earlier firmware release.

Notes

Processor Status File

Processor status data is stored in data file 2.

IMPORTANT For more information about any of these topics, see the description in this manual or the documentation for your programming software.

S:0 - S:2

This Word	Stores
S:0	Arithmetic flags • bit 0 = carry • bit 1 = overflow • bit 2 = zero • bit 3 = sign
S:1Processor status and flags	
S:1/00	RAM checksum is invalid at power-up
S:1/01	Controller in run mode
S:1/02	Controller in test mode
S:1/03	Controller in program mode
S:1/04	Controller uploading to memory module
S:1/05	Controller in download mode
S:1/06	Controller has test edits enabled
S:1/07	Mode select switch in REMOTE position
S:1/08	Forces enabled
S:1/09	Forces present
S:1/10	Controller controllerr successfully uploaded to memory module
S:1/11	Performing online programming
S:1/12	Not defined
S:1/13	User program checksum calculated
S:1/14	Last scan of ladder or SFC step
S:1/15	Controller running first program scan or the first scan of the next step in an SFC

This Word	Stores
S:2	Switch setting information
S:2/00 through S:2/05	Channel 1A DH+ station number
S:2/06	Channel 1A DH+ baud rate 057.6 kbps 1230.4 kbps
S:2/07 S:2/08	Not defined
S:2/09	Last state 0outputs are turned off 1outputs retain last state
S:2/11 S:2/12	I/O chassis addressing bit 12bit 11 00illegal 101/2-slot 011-slot 112-slot
S:2/13 S:2/14	Memory module transfer bit 14bit 13 00memory module transfers to controller memory if controller memory is not valid 01memory module does not transfer to controller memory 11memory module transfers to controller memory at powerup
S:2/15	Controllercontroller memory protection 0enabled 1disable

S:3-10

This Word	Stores
S:3 to S:6	Active Node table for channel 1A Word Bits DH+ Station # 30-1500-17 40-1520-37 50-1540-57 60-1560-77
S:7	Global status bits: (See also S:27, S:32, S:33, S:34, and S:35) • S:7/0-7 rack fault bits for racks 0-7 • S:7/8-15 unused
S:8	Last program scan (in ms)
S:9	Maximum program scan (in ms)
S:10	Minor fault (word 1) See also S:17
S:10/00	Battery is low (replace in 1-2 days)
S:10/01	DH+ active node table has changed
S:10/02	STI delay too short, interrupt program overlap
S:10/03	memory module transferred at power-up
S:10/04	Edits prevent SFC continuing; data table size changed during program mode; reset automatically in run mode
S:10/05	Invalid I/O status file
S:10/06	reserved
S:10/07	No more command blocks exist to execute block-transfers
S:10/08	Not enough memory on the memory module to upload the program from the controller
S:10/09	No MCP is configured to run
S:10/10	MCP not allowed
S:10/11	PII word number not in local rack
S:10/12	PII overlap
S:10/13	no command blocks exist to get PII
S:10/14	Arithmetic overflow
S:10/15	SFC “lingering” action overlap - step was still active when step was reactivated

S:11

This Word	Stores
S:11major fault word	
S:11/00	Corrupted program file (codes 10-19). See major fault codes (S:12).
S:11/01	Corrupted address in ladder program (codes 20-29). See major fault codes (S:12).
S:11/02	Programming error (codes 30-49). See major fault codes (S:12).
S:11/03	Controller detected an SFC fault (codes (71-79). See major fault codes (S:12).
S:11/04	Controller detected an error when assembling a ladder program file (code 70); duplicate LBLs found.
S:11/05	Start-up protection fault. The controller sets this major fault bit when powering up in Run mode if the user control bit S:26/1 is set.
S:11/06	Peripheral device fault
S:11/07	User-generated fault; controller jumped to fault routine (codes 0-9). See major fault codes (S:12).
S:11/08	Watchdog faulted
S:11/09	System configured wrong (codes 80-82, 84-88, 200-208). See major fault codes (S:12).
S:11/10	Recoverable hardware error
S:11/11	MCP does not exist or is not a ladder or SFC file
S:11/12	PII file does not exist or is not a ladder file
S:11/13	STI file does not exist or is not a ladder file
S:11/14	Fault routine does not exist or is not a ladder file
S:11/15	Faulted program file does not contain ladder logic

S:12

This word stores the following fault codes:

This Fault Code	Indicates this Fault	And the Fault Is
00-09	Reserved for user-defined fault codes. You can use user-defined fault codes to identify different types of faults or error conditions in your program by generating your own recoverable fault. To use these fault codes, choose an input condition that decides whether to jump to a fault routine file, then use the JSR instruction as the means to jump to the fault routine file. To use the JSR instruction, enter the fault code number 0-9 (an immediate value) as the first input parameter of the instruction. Any other input parameters are ignored (even if you have an SBR instruction at the beginning of your fault routine file. You cannot pass parameters to the fault routine file using JSR/SBR instructions). You do not have to use the user-defined fault codes to generate your own fault. If you program a JSR with no input parameters, the controller will write a zero to the Fault Code field. The purpose of using the user-defined fault codes is to allow you to distinguish among **different** types of faults or error codes based on the 0-9 fault code numbers. When the input condition is true, the controller copies the fault code number entered as the first input parameter of the JSR instruction into word 12 of the processor status file (S:12), which is the Fault Code field. The controller sets a Major Fault S:11/7 "User-Generated Fault." The controller then faults unless you clear the Major Fault word (S:11) or the specific fault bit via ladder logic in the fault routine.	Recoverable: The fault routine can instruct the controller to clear the fault and then resume scanning the program. A fault routine executes when any of these faults occur.
10	Run-time data table check failed	Recoverable: The fault routine can instruct the controller to clear the fault and then resume scanning the program. A fault routine executes when any of these faults occur.
11	Bad user program checksum	
12	Bad integer operand type, restore new controller memory file	
13	Bad mixed mode operation type, restore new controller memory file	
14	Not enough operands for instruction, restore new controller memory file	
15	Too many operands for instructions, restore new controller memory file	
16	Corrupted instruction, probably due to restoring an incompatible controller memory file (bad opcode)	
17	Can't find expression end; restore new controller memory file	
18	Missing end of edit zone; restore new controller memory file	
19	Download aborted	
20	You entered too large an element number in an indirect address	
21	You entered a negative element number in an indirect address	
22	You tried to access a non-existent program file	
23	You used a negative file number, you used a file number greater than the number of existing files, or you tried to indirectly address files 0, 1, or 2	
24	You tried to indirectly address a file of the wrong type	Recoverable

This Fault Code	Indicates this Fault	And the Fault Is
30	You tried to jump to one too many nested subroutine files	Non-recoverable The fault routine will be executed but cannot clear major fault bit 2.
31	You did not enter enough subroutine parameters	
32	You jumped to an invalid (non-ladder) file	
33	You entered a CAR routine file that is not 68000 code	
34	You entered a negative preset or accumulated value in a timer instruction	Recoverable
35	You entered a negative time variable in a PID instruction	
36	You entered an out-of-range setpoint in a PID instruction	
37	You addressed an invalid module in a block-transfer, immediate input, or immediate output instruction	
38	You entered a RET instruction from a non-subroutine file	Non-recoverable The fault routine will be executed but cannot clear major fault bit 2.
39	FOR instruction with missing NXT	
40	The control file is too small for the PID, BTR, BTW, or MSG instruction	Recoverable
41	NXT instruction with missing FOR	Non-recoverable The fault routine will be executed but cannot clear major fault bit 2.
42	You tried to jump to a non-existent label	
43	File is not an SFC	
44	Error using SFR. This error occurs if: • you tried to reset into a simultaneous path • you specified a step reference number that is not found or is not tied to a step (it is a transition) • the previous SFR to a different step is not complete	
45	Invalid channel number entered	Recoverable
46	Length operand of IDI or IDO instruction is greater than the maximum allowed	
47	SFC action overlap. An action was still active when the step became re-activated	Non-recoverable. The fault routine will be executed but cannot clear major fault bit 2.

This Fault Code	Indicates this Fault	And the Fault Is
70	The controller detected duplicate labels	Non-recoverable
71	The controller tried to start an SFC subchart that is already running	
72	The controller tried to stop an SFC subchart that isn't running	
73	The controller tried to start more than the allowed number of subcharts	
74	SFC file error detected	
75	The SFC has too many active functions	
76	SFC step loops back to itself.	
77	The SFC references a step, transition, subchart, or SC file that is missing, empty or too small	
78	The controller cannot continue to run the SFC after power loss	
79	You tried to download an SFC to a controller that cannot run SFCs	
80	You have an I/O configuration error	
81	You illegally set an I/O chassis backplane switch by setting both switch 4 and 5 on	
82	Illegal cartridge type for selected operation. This error also occurs if the controller doesn't have a memory module, but the backplane switches are set for a memory module. Make sure the backplane switches are correct (set switch 6 ON and switch 7 OFF if the controller doesn't have a memory module).	
83	User watchdog fault	Recoverable
84	Error in user-configured adapter mode block-transfer	Non-recoverable
85	Memory module bad	
86	Memory module is incompatible with host	Non-recoverable
87	Scanner rack list overlap	
88	Scanner channels are overloading the remote I/O buffer; too much data for the controller to process. If you encounter fault code 88, be sure you followed the design guidelines listed on page 4-9. Specifically, make sure you: • group together 1/4-racks and 1/2-racks of each logical rack. Do not intersperse these with other rack numbers • if using complementary I/O addressing, treat complementary rack addresses individually when grouping racks; primary rack numbers are separate from complement rack numbers	

This Fault Code	Indicates this Fault	And the Fault Is
90	Sidecar module extensive memory test failed. Call your Allen-Bradley representative for service	Recoverable
91	Sidecar module undefined message type	
92	Sidecar module requesting undefined pool	
93	Sidecar module illegal maximum pool size	
94	Sidecar module illegal ASCII message	
95	Sidecar module reported fault, which may be the result of a bad sidecar program or of a hardware failure	
96	Sidecar module not physically connected to the PLC-5 controller	
97	Sidecar module requested a pool size that is too small for PC^3 command (occurs at power-up)	
98	Sidecar module first/last 16 bytes RAM test failed	
99	Sidecar module-to-controller data transfer faulted	
100	Controller-to-sidecar module transfer failed	
101	Sidecar module end of scan transfer failed	
102	The file number specified for raw data transfer through the sidecar module is an illegal value	
103	The element number specified for raw data transfer through the sidecar module is an illegal value	
104	The size of the transfer requested through the sidecar module is an illegal size	
105	The offset into the raw transfer segment of the sidecar module is an illegal value	
106	Sidecar module transfer protection violation; for PLC-5/26, -5/46, and -5/86 controllers only	

S:13-S:24

This Word:	Stores
S:13	Program file where fault occurred
S:14	Rung number where fault occurred
S:15	VME status file
S:16	I/O status File
S:17	Minor fault (word 2) See also S:10.
S:17/00	BT queue full to remote I/O
S:17/01	Queue full - channel 1A; maximum remote block-transfers used
S:17/02	Queue full - channel 1B; maximum remote block-transfers used
S:17/03	Queue full - channel 2A; maximum remote block-transfers used
S:17/04	Queue full - channel 2B; maximum remote block transfers used
S:17/05	No modem on serial port
S:17/06	• Remote I/O rack in local rack table or • Remote I/O rack is greater than the image size. This fault can also be caused by the local rack if the local rack is set for octal density scan and the I/O image tables are smaller than 64 words (8 racks) each.
S:17/07	Firmware revision for channel pairs 1A/1B or 2A/2B does not match controller firmware revision
S:17/08	ASCII instruction error
S:17/09	Duplicate node address
S:17/10	DF1 master poll list error
S:17/11	Protected controller data table element violation
S:17/12	Protected controller file violation
S:17/13	Using all 32 ControlNet MSGs
S:17/14	Using all 32 ControlNet 1771 READ and/or 1771 WRITE CIOs
S:17/15	Using all 8 ControlNet Flex I/O CIOs
S:18	Controller clock year
S:19	Controller clock month
S:20	Controller clock day
S:21	Controller clock hour
S:22	Controller clock minute
S:23	Controller clock second
S:24	Indexed addressing offset
S:25	Reserved

S:26-S:35

This Word	Stores
S:26	User control bits
S:26/00	Restart/continuous SFC: when reset, controller restarts at first step in SFC. When set, controller continues with active step after power loss or change to RUN
S:26/01	Start-up protection after power loss: when reset, no protection. When set, controller sets major fault bit S:11/5 when powering up in run mode.
S:26/02	Define the address of the local rack: when reset, local rack address is 0. When set, local rack address is 1.
S:26/03	Set complementary I/O (series A only): when reset, complementary I/O is not enabled. When set, complementary I/O is enabled.
S:26/04	Local block-transfer compatibility bit: when reset, normal operation. When set, eliminates frequent checksum errors to certain BT modules.
S:26/05	PLC-3 scanner compatibility bit: when set (1), adapter channel response delayed by 1 ms; when reset (0) operate in normal response time.
S:26/06	Data table-modification inhibit bit. When set (1), user cannot edit the data table or modify forces while the controller keyswitch is in the RUN position. You control this bit with your programming software
S:26/07 through S:26/15	Reserved
S:27	Rack control bits: (See also S:7, S:32, S:33, S:34, and S:35) • S:27/0-7 - - I/O rack inhibit bits for racks 0-7 • S:27/8-15 - - I/O rack reset bits for racks 0-7
S:28	Program watchdog setpoint
S:29	Fault routine file
S:30	STI setpoint
S:31	STI file number
S:32	Global status bits: (See also S:7, S:27, S:33, S:34, and S:35) • S:32/0-7 rack fault bits for racks 10-17 (octal) • S:32/8-15 unused
S:33	Rack control bits: (See also S:7, S:27, S:32, S:34, and S:35) • S:33/0-7 I/O rack inhibit bits for racks 10-17 • S:33/8-15 I/O rack reset bits for racks 10-17
S:34	Global status bits: (See also S:7, S:27, S:32, S:33, and S:35) • S:34/0-7 rack fault bits for racks 20-27 (octal) • S:34/8-15 unused
S:35	Rack control bits: (See also S:7, S:27, S:32, S:33, and S:34) • S:35/0-7 I/O rack inhibit bits for racks 20-27 • S:35/8-15 I/O rack reset bits for racks 20-27

IMPORTANT Setting inhibit bits in the processor status file (S:27, S:33, or S:35) does not update inhibit bits in the I/O status file.

S:36-S:78

This Word	Stores
S:36 - S:45	Reserved
S:46	PII program file number
S:47	PII module group
S:48	PII bit mask
S:49	PII compare value
S:50	PII down count
S:51	PII changed bit
S:52	PII events since last interrupt
S:53	STI scan time (in ms)
S:54	STI maximum scan time (in ms)
S:55	PII last scan time (in ms)
S:56	PII maximum scan time (in ms)
S:57	User program checksum
S:58	Reserved
S:59	Extended-local I/O channel discrete transfer scan (in ms)
S:60	Extended-local I/O channel discrete maximum scan (in ms)
S:61	Extended-local I/O channel block-transfer scan (in ms)
S:62	Extended-I/O channel maximum block-transfer scan (in ms)
S:63	Protected controller data table protection file number
S:64	The number of remote block-transfer command blocks being used by channel pair 1A/1B.
S:65	The number of remote block-transfer command blocks being used by channel pair 2A/2B.
S:66	Reserved.

This Word	Stores
S:68	Installed memory card type: 0 - No memory card installed 1 - 1785-ME16 2 - 1785-ME32 3 - 1785-ME64 4 - 1785-ME100 5 - 1785-CHBM 6 - 1785-RC 7-15 - Reserved When the 1785-RC module is installed, the eight least-significant bits indicate the memory card's status: Bit 3 is set when the memory card is installed Bit 2 is set when contact is detected closed Bit 1 is set when the relay is driven open Bit 0 is set when 120V ac is present on the memory card When any other memory card is installed, the bits are undefined.
S:77	Communication time slice for communication housekeeping functions (in ms)
S:78	MCP I/O update disable bits Bit 0 for MCP A Bit 1 for MCP B etc.

S:79-S:127

This Word	Stores
S:79	MCP inhibit bits Bit 0 for MCP A Bit 1 for MCP B etc.
S:80-S:127	MCP file number MCP scan time (in ms) MCP max scan time (in ms) The above sequence applies to each MCP; therefore, each MCP has 3 status words. For example,word 80: file number for MCP A word 81: scan time for MCP A word 82: maximum scan time for MCP A word 83: file number for MCP B word 84: scan time for MCP B etc.

Maximizing System Performance

Using This Chapter

For information about the time that it takes the controller to execute a specific instruction, see Appendix D.

Program Scan

Since the program scan is comprised of the logic scan and housekeeping, any event that impacts the time of one segment affects the program scan.

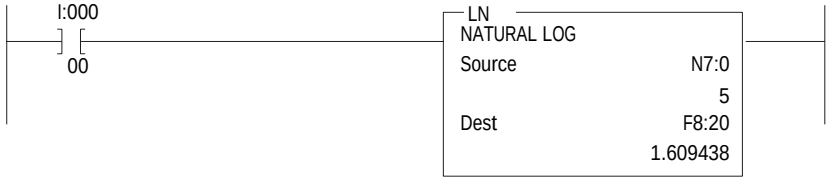
You can monitor the scan time by using the controller status screen in your programming software.

If no change in input status occurs and the controller continues to execute the same ladder logic instructions, the program scan cycle is consistent. In real systems, however, the program scan cycle fluctuates due to the following factors:

- false logic executes faster than true logic
- different instructions execute at different rates
- different input states cause different sections of logic to be executed
- interrupt programs affect program scan times
- editing programs while online affects housekeeping times

Effects of False Logic versus True Logic on Logic Scan Time

The rung below—which changes states from one program scan to the next—will change your scan time by about 400 µs.

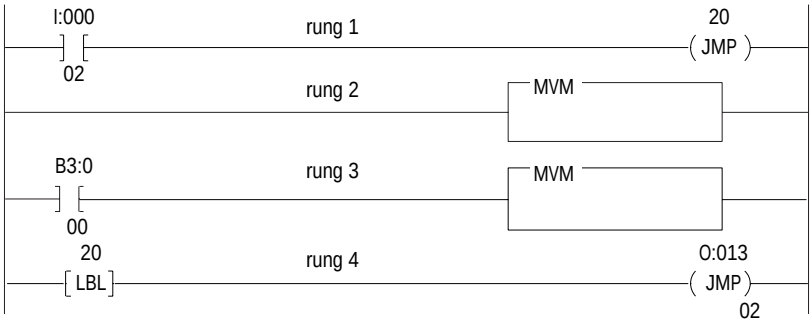


If I:000/00 is	Then the Rung is
On	True, and the controller calculates the natural log. A natural log instruction takes 409 µs to execute.
Off	False, and the controller scans the rung but does not execute it. It takes only 1.4 µs to only scan the rung.

Other instructions may have a greater or lesser effect.

Effects of Different Input States on Logic Scan Time

You can write your logic so that it executes different rungs at different times, based on input conditions. The amount of logic executed in logic scans causes differences in program scan times. For example, the simple differences in rung execution in the following example cause the program scan to vary.



If I:000/02 is	Rungs 2 and 3 are
On	Skipped
Off	Executed

If you use subroutines, program scan times can vary by the scan time of entire logic files.

Effects of Different Instructions on Logic Scan Time

Some instructions have a much greater effect on logic scan time than others based on the time that it takes to execute each instruction.

Program scan time is also affected by the construction of your ladder rungs. The size of the rung and the number of branches can cause the scan time to fluctuate greatly.

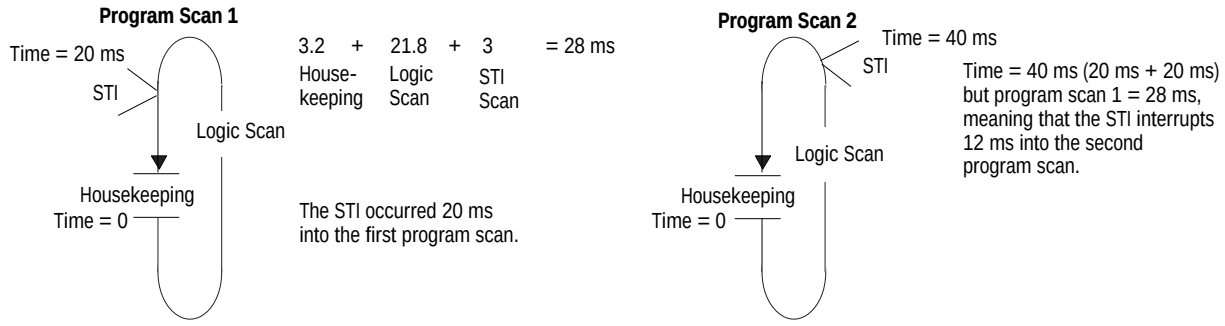
Effects of Using Interrupts on Logic Scan Time

Program scan time is also affected by interrupt programs. An interrupt is a special situation that causes a separate program to run independently from the normal program scan. You define the special event and the type of interrupt that is to occur. For more information on interrupt programs, see chapters 18 and 19.

For example, a selectable timed interrupt (STI) is a program file that you define to execute once every time period. The example shown below has these parameters:

- you configure an STI to execute every 20 ms
- the STI program takes 3 ms to execute
- the logic scan is 21.8 ms
- housekeeping takes 3.2 ms

The first program scan in this example lasts a total of 28 ms. The program scans look like:



Because the first program scan takes 28 ms, the STI actually occurs 12 ms into the second program scan (28 + 12 = 40, which is the time for the second STI to occur). This example points out that when the STI time period is different than the program scan time, the STI occurs in different places in the program scan. Also note that, due to fluctuations in program-scan times, multiple STIs may be executed during one scan and no STIs during other scans.

Effects of Housekeeping Time

In PLC-5 controllers, basic housekeeping takes 3.5 ms. If it takes the controller 21.8 ms to execute a ladder program, the overall program scan time is 25.3 ms. Any increase in housekeeping affects your program scan.

The following activities can increase housekeeping time:

- editing while in remote run mode
- putting block-transfer modules in the controller-resident chassis
- using the global status flag files

Editing While in Remote Run Mode

The online editing times for ladder programs are as follows:

For this Editing Operation	And this Type of Program	The Times are
Accept Rung (after inserting, modifying, or deleting a rung edit)	other than the edited file	0.35 ms per 1000 words
	no labels	3 ms + 0.35 ms per 1000 words
	with labels	3.5 ms + 0.35 ms per 1000 words
Test Edits of the program (impacts one program scan)		0.2 ms to change the status of edits from TEST to UNTEST or UNTEST to TEST
Assemble Edits	no edits pending	0.35 ms per 1000 words
	edits pending, no labels	2.0 ms + 1.5 ms per 1000 words
	edits pending, with labels	2.0 ms + 1.9 ms per 1000 words

IMPORTANT Editing programs online also delays the execution of PIIs and STIs.

Putting Block-Transfer Modules in Controller-Resident Chassis

Because controller-resident racks cannot be updated until after active block-transfers are completed, putting block-transfer modules in the controller-resident chassis can affect housekeeping by a worst-case time of approximately 100 µs per one word of block-transfer data. Note that this estimate is based on a worst-case scenario. Typically, the effect, if any, on housekeeping will be minimal.

Using Global Status Flag Files

The global status flag files are updated during housekeeping. This increases housekeeping time as follows:

- each global status flag file on a channel (for example, channel 1A or 1B) adds 3ms
- housekeeping time does not increase more than 6ms, even if there are more than two global status flag files

If you need two global status flag files, split them across two channels.

Calculating Throughput

Throughput is the time that it takes for an output to be energized after its associated input has been energized. You need to consider the following components when evaluating throughput:

- input and output module delay
- I/O backplane transfer
- remote I/O scan time
- controller time

To calculate throughput, use the following equation:

Input Card Delay	+	I/O Backplane	+	Worst-Case Remote I/O Scan Time	+	Worst-Case Processor Time	+	Worst-Case Remote I/O Scan Time	+	I/O Backplane	+	Output Card Delay

Input and Output Modules Delay

All input and output modules have a “delay time,” which is the time that it takes the module to transfer information to/from the I/O backplane through the I/O module to/from the field device.

Depending on the type of modules you are using, these delay times vary; but, the times must be taken into account when calculating system throughput. Choose modules that perform the function that you need with the lowest possible delay times.

I/O Backplane Transfer

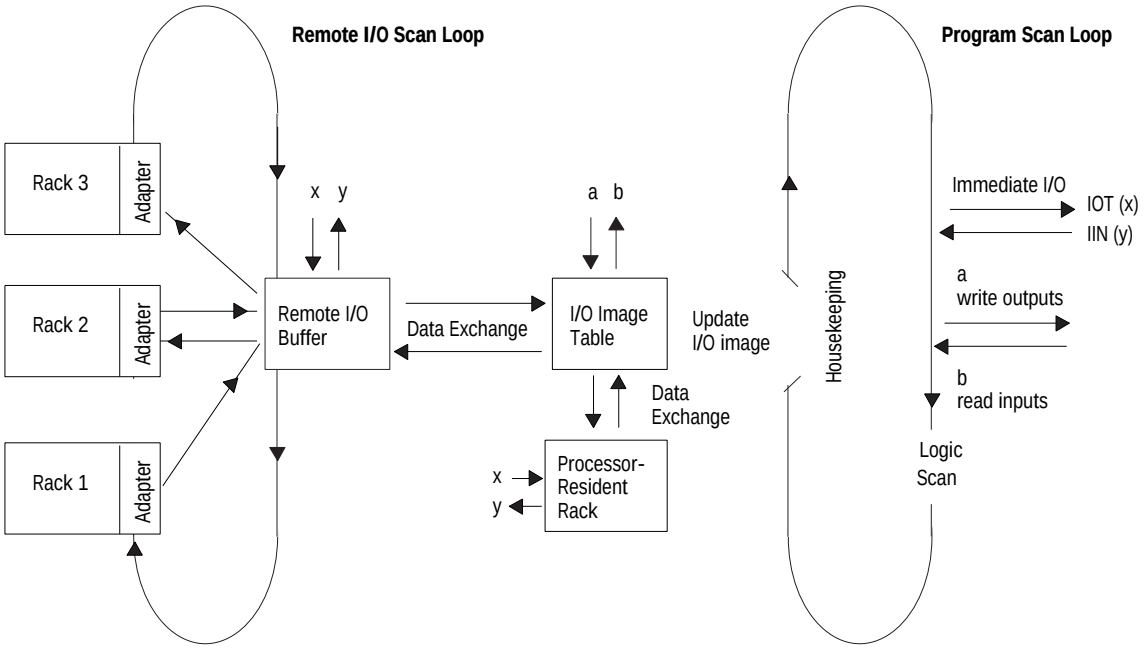
The I/O backplane transfer time is the time it takes for the 1771-ASB adapter module to exchange data with the I/O modules in the same chassis, generally 1-2 ms for a full I/O rack.

This time is fairly insignificant compared to total system throughput, but can be optimized in situations where empty slots or modules that use only backplane power in the chassis exist. For example, if the last four slots of a rack contain a 1785-KA module and power supply (with two empty slots), the 1771-ASB can be configured to ignore those last four slots.

For more information about configuring adapter modules, see the 1771 Remote I/O Adapter Module User Manual, publication 1771-UM001.

Remote I/O Scan Time

The remote I/O scan time is the time it takes for the scanner to communicate with each device in the remote I/O system.



These three factors affect the remote I/O scan time:

- communication rate
- number of rack entries
- block-transfers

Communication Rate

The communication rate determines the time it takes for the scanner to communicate with each individual entry in its scan list. The following table lists the amount of time required to communicate to a device at each communication rate.

Communication Rate (kbps):	Time (ms):
57.6	10
115.2	7
230.4	3

Note that these are full rack times. Smaller racks will decrease this time.

If four full-rack entries are in the scan list, the I/O scan for that channel at 57.6 kbps is 4 x 10 = 40 ms. If you change the communication rate to 230.4 kbps, the I/O scan decreases to
4 x 3 = 12 ms.

Number of Rack Entries

You determine the total remote I/O scan time in the remote I/O system by this formula:

total remote I/O scan time = # of rack entries X time per rack-entries in the scan list (see on page 7)

If one channel has twice as many racks as another, for example, the scan time for the first channel is twice as long.

To optimize this scan time, divide your I/O racks between multiple channels. Place your most time-critical I/O on one channel, and non- time-critical I/O on the other channel. Since all I/O channels are independent, a long remote I/O scan on one channel will not affect the remote I/O scan on another channel.

Block-Transfers

A block-transfer is an interruption of the normal remote I/O scan in order to transfer a block of data to a specific I/O module. Most of the time that the controller spends in performing the block-transfer is for the handshaking that occurs between the controller and the block-transfer module. This handshaking is embedded in the discrete I/O transfer and has no effect on the remote I/O scan. The remote I/O scan is affected when the actual data transfer occurs.

The amount of time that the block-transfer interrupts the remote I/O scan depends on the number of words being transferred, the communication rate, and associated overhead:

Use this formula and the table below to calculate block-transfer time:

block-transfer time = (number of words being transferred ms/word based on the communication rate) + overhead for the communication rate

Communication Rate (kbps)	ms/Word	Overhead (ms)
57.6	.28	3
115.2	.14	2.5
230.4	.07	2

For example, if the communication rate is 115.2 kbps and you want to block-transfer 10 words, the interruption of the remote I/O scan is:

(10 x .14) + 2.5 = 1.4 + 2.5 = 3.9 ms

For the particular remote I/O scan in which the block-transfer takes place, 3.9 ms will be added to the remote I/O scan time.

IMPORTANT If you select the baud rate as 230.4 kbps, and you are using the serial port or a PLC-5 coprocessor, use channel 2 for better overall system performance.

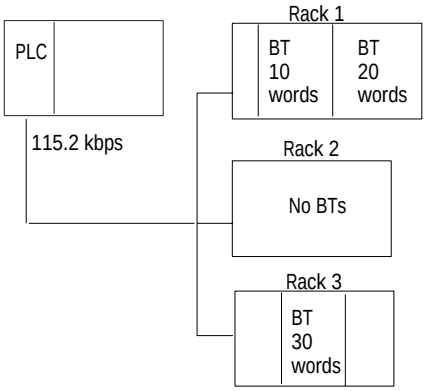
Calculating Worst-Case Remote I/O Scan Time

Since it is impossible to predict within which remote I/O scan a block-transfer will occur, you only can calculate the worst-case remote I/O scan time. To calculate the worst case time:

1. Determine the normal I/O time (without block-transfers)

2. Add the time of the longest block-transfer to each entry in the scan list. (The controller can only perform one block-transfer per entry in the scan list per I/O scan.)

For example, if your system is:



Worst-case I/O scan:

(3 x 6)	3 racks at 115.2 kbps*normal I/O scan
+ (20 x .14) + 2.5	longest BT in rack 1
+ 0	no BTs in rack 2
+ (30 x .14) + 2.5	longest BT in rack 3

18 + 5.3 + 0 + 6.7 = 30 ms

Optimizing Remote I/O Scan Time

The best way to optimize your scan time is to place your most time-critical I/O on a separate channel from non-critical I/O. If you have only one channel available for I/O, however, you can still optimize the scanning by using the controller's configurable scan list.

In a normal 4-rack system, the scan list would be:
rack 1
rack 2
rack 3
rack 4

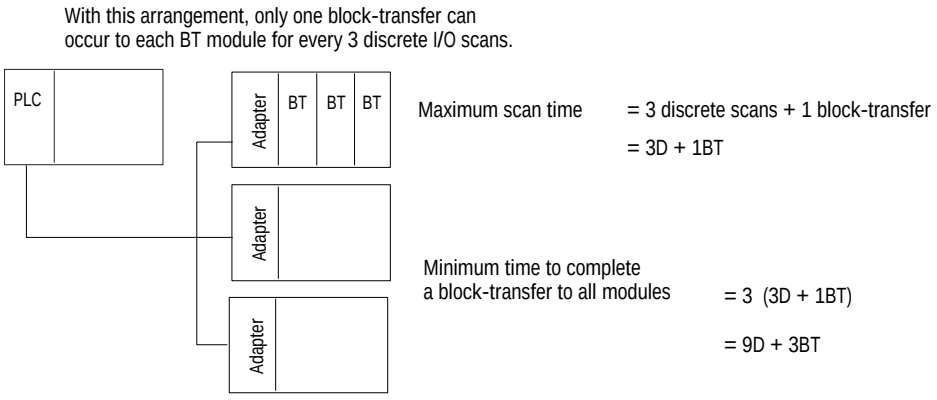
If you are using 57.6 kbps, the normal I/O scan is 4 racks x 10 ms = 40 ms. Each entry is of equal priority, so each rack is scanned every 40 ms.

However, if rack 2 has the most time-critical I/O, use the configurable scan list to specify:
rack 1
rack 2
rack 3
rack 2
rack 4
rack 2

Using this scan list, rack 2 is scanned every other rack. The list has 6 entries, so the normal I/O scan time is 6 x 10 ms = 60 ms. Since rack 2 is scanned every other rack, however, the rack 2 **effective** scan time is 2 x 10 ms = 20 ms. The remaining racks are scanned every 60 ms. Thus, the tradeoff for the more frequent scanning of rack 2 (every 20 ms) means that the other racks are scanned only every 60 ms.

You can also optimize block-transfers within the channel. You block-transfer to only one block-transfer module per entry in the scan list per I/O scan. If you have three block-transfer modules in one I/O rack, it takes a minimum of three I/O scans to complete the block-transfers to all of the modules:

System Optimized for Discrete-Data Transfer

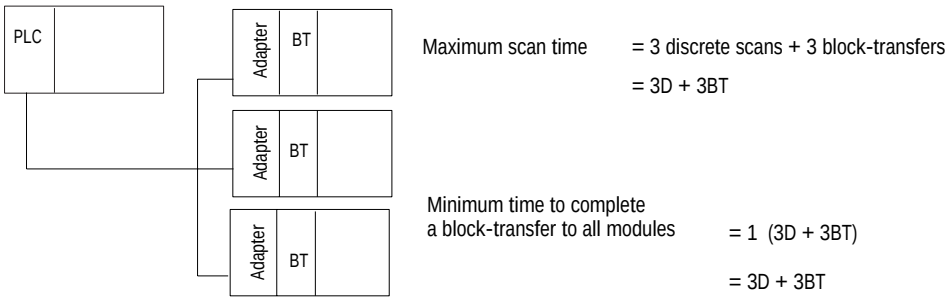


If you place the three block-transfer modules in different racks, however, you can block-transfer to all three modules in one I/O scan.

To optimize your system layout for block-data transfers, use an arrangement similar to the following:

System Optimized for Block-Data Transfer

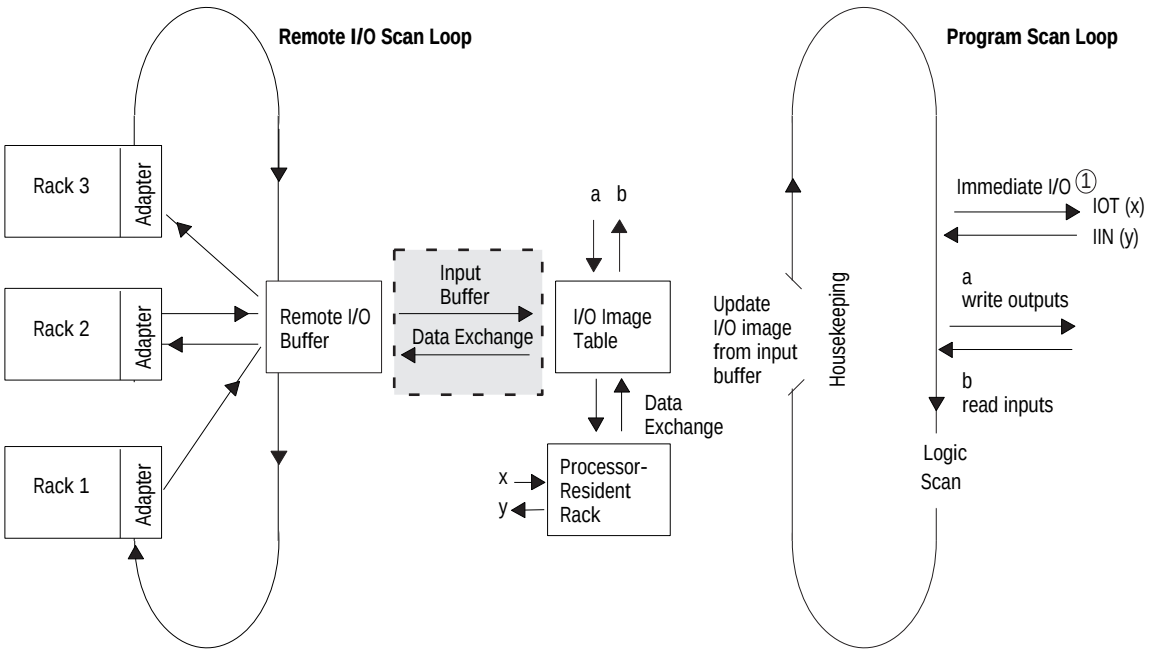
With this arrangement, a block-transfer to each BT module can occur in a single discrete I/O scan.



Controller Time

The controller time is the time needed to process the inputs and set the corresponding outputs. This controller time varies for different controllers and is based on input buffering, program scan, etc.

In a PLC-5 system, inputs are buffered between the I/O image table and the remote I/O buffer. The movement of inputs from the remote I/O buffer to the input buffer is asynchronous to the movement of data from the input buffer to the input image table.



The worst-case controller time is:

Variable	Value
periodic input buffer update from remote I/O buffer	10 ms
one program scan to guarantee inputs received	xx ms
one program scan to guarantee outputs received	xx ms
0.18 ms times number of racks	xx ms
total	

For a 3-rack system with a 20 ms program scan, the worst-case controller time is: $10 + 20 + 20 + (0.18 * 3) = 50.54$ ms.

Example Calculation

Based on the results of each throughput component calculation presented within the chapter, an example of a worst-case update time calculation is:

Variable	Value
input card delay	10 ms typical
I/O backplane	1 ms
worst-case remote I/O scan time	30 ms
worst-case controller time	50.54 ms
worst-case remote I/O scan time	30 ms
I/O backplane	1 ms
output card delay	1 ms typical
total	123.54 ms

Performance Effects of Online Operations

The performance of the PLC-5 controller is affected when you perform online operations via a DH+ link to your program files while in Run mode. Affected activities are:

- DH+ messages
- serial port messages
- channel 3A messages
- remote block-transfers

The amount of time that the messaging and block-transfers can be delayed is **proportional to the size (K words) of the ladder file**. The following table lists the performance effects (when using any of the 6200 Series PLC-5 Programming Software releases that support the controller you are using).

Effected Data Transfers	Online Operations via any DH+ Channel:	
	Perform a Page Up/Page Down at the End of a Program File	Insert/Delete Ladder Rungs
Remote block-transfers	20 ms/K words	50 ms/Kwords
DH+ messages	20 ms/K words	50 ms/Kwords
Serial port messages	200 ms/K words	50 ms/Kwords
Channel 3A messages	no impact	50 ms/Kwords

You should re-design your programs to avoid possible communication pauses if you currently:

- use large ladder logic program files
- have time critical remote block-transfers and/or serial, DH+, and channel 3A messages
- must edit the program online during run mode

For best controller performance, segment your program files by using modular programming design practices, such as main control programs (MCPs), sequential function charts (SFCs), and the jump to subroutine (JSR) instruction.

Effect of Inserting Ladder Rungs at the 56K-word Limit

This consideration applies to PLC-5/60, -5/60L, -5/80, and -5/80E controllers when you are editing a program file that approaches the maximum file limit of 57,344 words.

Performing run-time or program-mode editing of ladder files that approach the maximum program file size of 57,344 words could:

- prevent the rung from being inserted
- cause suspension of the operation by 6200 Series PLC-5 Programming Software (release 4.3 and later)

To avoid or correct this problem, segment your program file using modular programming, such as main control programs (MCPs), sequential function charts (SFCs), and the jump to subroutine (JSR) instruction.

If you cannot segment your program file, save the file often while editing it.

If you encounter the error `Memory Unavailable for Attempted Operation`, then clear controller memory.

Using Program Control Instructions

Scan time can increase based on how you use JMP/LBL instructions and FOR/NXT instructions.

Using JMP/LBL Instructions

Keep in mind these issues when programming JMP/LBL instructions:

Instruction	Consideration
JMP	The execution time required for a JMP instruction depends on the program file that contains the JMP instruction. The estimated execution time for a JMP instruction is: 8.9 + (*file_number* – 2) ∗ 0.96 The greater the program file number, the longer it takes to complete a scan of the JMP instruction.
LBL	Each LBL instruction uses 2 words of memory in the program file plus additional memory, depending on the label number itself. Each label number is placed in a label table. Each entry in the label table uses 2 words of memory, starting from label 0. For example, LBL 10 uses 22 (2 words ∗ 11th entry) words of memory in the label table. If you later delete LBL 10, the label table does not deallocate previously used space. The only way to recover this space is to upload and then re-download the program.

Using FOR/NXT Instructions

The FOR/NXT instructions have the same impact on execution time as the JMP instruction. The execution for a FOR/NXT loop depends on the program file that contains the instructions.

The estimated execution time for a FOR/NXT loop is:
8.1 + (number_of_loops ∗ 15.9) + (file_number – 2) ∗ 0.96

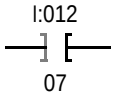
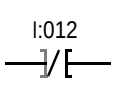
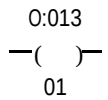
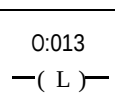
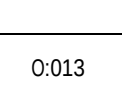
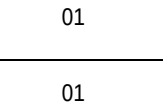
The greater the program file number, the longer it takes to complete the FOR/NXT loops.

Instruction Set Quick Reference

Using This Chapter

IMPORTANT For a more detailed description of each of these instructions, see the PLC-5 Programming Software Instruction Set Reference, publication 1785-6.1.

Relay Instructions

Instruction		Description
	Examine On XIC	Examine data table bit I:012/07, which corresponds to terminal 7 of an input module in I/O rack 1, I/O group 2. If this data table bit is set (1), the instruction is true.
	Examine Off XIO	Examine data table bit I:012/07, which corresponds to terminal 7 of an input module in I/O rack 1, I/O group 2. If this data table bit is reset (0), the instruction is true.
	Output Energize OTE	If the input conditions preceding this output instruction on the same rung go true, set (1) bit O:013/01, which corresponds to terminal 1 of an output module in I/O rack 1, I/O group 3.
	Output Latch OTL	If the input conditions preceding this output instruction on the same rung go true, set (1) bit O:013/01, which corresponds to terminal 1 of an output module in I/O rack 1, I/O group 3. This data table bit remains set even if the rung condition goes false.
	Output Unlatch OTU	If the input conditions preceding this output instruction on the same rung go true, reset (0) bit O:013/01, which corresponds to terminal 1 of an output module in I/O rack 1, I/O group 3. This is necessary to reset a bit that has been latched on.
	Immediate Input IIN	This instruction updates a word of input-image bits before the next normal input-image update. Address this instruction by rack and group (RRG). For a local chassis, program scan is interrupted while the inputs of the addressed I/O group are scanned; for a remote chassis, program scan is interrupted only to update the input image with the latest states as found in the remote I/O buffer.
	Immediate Output IOT	This instruction updates a word of output-image bits before the next normal output-image update. Address this instruction by rack and group (RRG). For a local chassis, program scan is interrupted while the outputs of the addressed I/O group are updated; for a remote chassis, program scan is interrupted only to update the remote I/O buffer with the latest states as found in the output image.

Timer Instructions

Instruction		Description
TON TIMER ON DELAY Timer T4:1 Time Base 1.0 Preset 15 Accum 0	Timer On Delay TON Status Bits: EN - Enable TT - Timer Timing DN - Done	If the input conditions go true, timer T4:1 starts incrementing in 1-second intervals. When the accumulated value is greater than or equal to the preset value (15), the timer stops and sets the timer done bit. Rung Condition / EN 15 / TT 14 / DN 13 / ACC Value / TON Status False / 0 / 0 / 0 / 0 / Reset True / 1 / 1 / 0 / increase / Timing True / 1 / 0 / 1 / >= preset / Done See page F-8 for a description of prescan operation for this instruction.
TOF TIMER OFF DELAY Timer T4:1 Time Base .01 Preset 180 Accum 0	Timer Off Delay TOF Status Bits: EN - Enable TT - Timer Timing DN - Done	If the input conditions are false, timer T4:1 starts incrementing in 10 1-ms intervals as long as the rung remains false. When the accumulated value is greater than or equal to the preset value (180), the timer stops and resets the timer Rung Condition / EN 15 / TT 14 / DN 13 / ACC Value / TOF Status True / 1 / 0 / 1 / 0 / Reset False / 0 / 1 / 1 / increase / Timing False / 0 / 0 / 0 / >= preset / Done See page F-8 for a description of prescan operation for this instruction.

Instruction		Description
RTO RETENTIVE TIMER ON Timer T4:10 Time Base 1.0 Preset 10 Accum 0	Retentive Timer On RTO Status Bits: EN - Enable TT - Timer Timing DN - Done	If the input conditions go true, timer T4:10 starts incrementing i 1-second intervals as long as the rung remains true. When the rung goes false, the timer stops. If the rung goes true again, th timer continues. When the accumulated value is greater than c equal to the preset (10), the timer stops and sets the timer don bit.

Rung Condition	EN 15	TT 14	DN 13	ACC Value	RTO Status
False	0	0	0	0	Disabled
True	1	1	0	increase	Timing
False	0	0	0	maintains	Disabled
True	1	0	1	>= preset	Done

T4:1 (RES)	Timer Reset RES	If the input conditions go true, timer T4:1 is reset. This instruction resets timers and counters, as well as control blocks. This is necessary to reset the RTO accumulated value.

Counter Instructions

Instruction		Description
CTU COUNT UP Counter C5:1 Preset 10 Accum 0	Count Up CTU Status Bits: CU-Count Up CD-Count Down DN-Count Up done OV-Overflow UN-Underflow	If the input conditions go true, counter C5:1 starts counting, incrementing by 1 every time the rung goes from false-to-true. When the accumulated value is greater than or equal to the preset value (10), the counter sets the counter

Rung Condition	CU 15	DN 13	OV 12	ACC Value	CTU Status
False	0	0	0	0	Disabled
Toggle True	1	0	0	incr by 1	Counting
True	1	1	0	>= preset	Done
True	1	1	1	>32767	Overflow

See page F-8 for a description of prescan operation for this instruction.

Instruction	Description
CTD COUNT DOWN Counter C5:1 Preset 10 Accum 35	Count Down CTD Status Bits: CU-Count Up CD-Count Down DN-Count Down done OV-Overflow UN-Underflow

If the input conditions go true, counter C5:1 starts counting, decrementing by 1 every time the rung goes from false-to-true. When the accumulated value is less than the preset value (10), the counter resets the counter done bit.

Rung Condition	CD 14	DN 13	UN 11	ACC Value	CTD Status
False	0	0	0	0	Disabled
False	0	1	0	>= preset	Preload
Toggle True	1	1	0	dec by 1	Counting
True	1	0	0	< preset	Done
True	1	0	1	< -32768	Underflow

See page F-8 for a description of prescan operation for this instruction.

Compare Instructions

Instruction	Description
LIM LIMIT TEST (CIRC) Low limit N7:10 3 Test N7:15 4 High limit N7:20 22	Limit Test LIM

If the Test value (N7:15) is >= the Low Limit (N7:10) and <= the High Limit (N7:20), this instruction is true.

Low Limit	Test	High Limit	LIM
0	0	10	T
-5	5	10	T
5	11	10	F
10	0	0	T
10	5	-5	F
10	11	5	T

Instruction	Description
MEQ MASKED EQUAL Source D9:5 0000 Mask D9:6 0000 Compare D9:10 0000	Mask Compare Equal MEQ

The controller takes the value in the Source (D9:5) and passes that value through the Mask (D9:6). Then the controller compare the result to the Compare value (D9:10). If the result and this comparison values are equal, the instruction is true.

Source	Mask	Compare	MEQ
0008	0008	0009	T
0008	0001	0001	F
0087	000F	0007	T
0087	00F0	0007	F

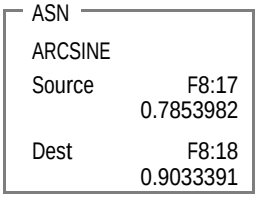
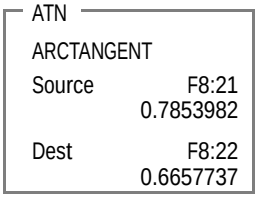
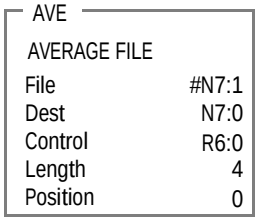
Instruction		Description
CMP COMPARE Expression N7:5 = N7:10	Compare CMP	If the expression is true, this input instruction is true. The CMP instruction can perform these operations: equal (=), less than (<), less than or equal (<=), greater than (>), greater than or equal (>=), not equal (<>), and complex expressions (up to 80 characters).
xxx xxxxxxxxxxxx Source A N7:53 Source B N7:101		

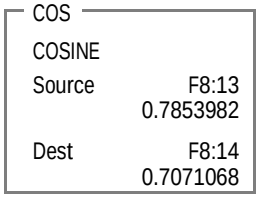
Source A	Source B	EQU	GEQ	GRT	LEQ	LES	NEQ
10	10	T	T	F	T	F	F
5	6	F	F	F	T	T	T
21	20	F	T	T	F	F	T
-30	-31	F	T	T	F	F	T
-15	-14	F	F	F	T	T	T

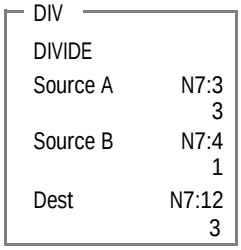
Equal to EQU	If the value in Source A (N7:5) is = to the value in Source B (N7:10), this instruction is true.
Greater than or Equal GEQ	If the value in Source A (N7:5) is > or = the value in Source B (N7:10), this instruction is true.
Greater than GRT	If the value in Source A (N7:5) is > the value in Source B (N7:10), this instruction is true.
Less than or Equal LEQ	If the value in Source A (N7:5) is < or = the value in Source B (N7:10), this instruction is true.
Less than LES	If the value in Source A (N7:5) is < the value in Source B (N7:10), this instruction is true.
Not Equal NEQ	If the value in Source A (N7:5) is not equal to the value in Source B (N7:10), this instruction is true.

Compute Instructions

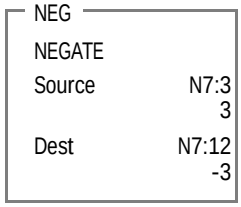
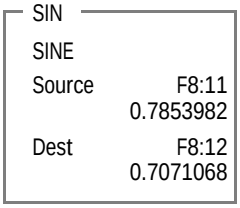
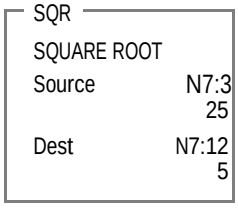
Instruction	Description
CPT COMPUTE Dest N7:3 3 Expression N7:4 - (N7:6 * N7:10) Compute CPT	If the input conditions go true, evaluate the Expression N7:4 - (N7:6 * N7:10) and store the result in the Destination (N7:3). The CPT instruction can perform these operations: add (+), subtract (-), multiply (*), divide (|), convert from BCD (FRD), convert to BCD (TOD), square root (SQR), logical and (AND), logical or (OR), logical not (NOT), exclusive or (XOR), negate (-) clear (0), and move, X to the power of Y (**), radians (RAD), degrees (DEG), log (LOG), natural log (LN), sine (SIN), cosine (COS), tangent (TAN), inverse sine (ASN), inverse cosine (ACS) inverse tangent (ATN), and complex expressions (up to 80 characters)
ACS ARCCOSINE Source F8:19 0.7853982 Dest F8:20 0.6674572 Arc cosine ACS	If input conditions go true, take the arc cosine of the value in F8:19 and store the result in F8:20. Status Bit / Description C — always resets V — sets if overflow is generated; otherwise resets Z — sets if the result is zero; otherwise resets S — always resets
ADD ADD Source A N7:3 3 Source B N7:4 1 Dest N7:12 4 Addition ADD	When the input conditions are true, add the value in Source A (N7:3) to the value in Source B (N7:4) and store the result in the Destination (N7:12). Status Bit / Description C — sets if carry is generated; otherwise resets V — sets if overflow is generated; otherwise resets Z — sets if the result is zero; otherwise resets S — sets if the result is negative; otherwise resets

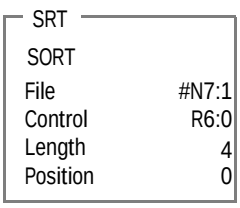
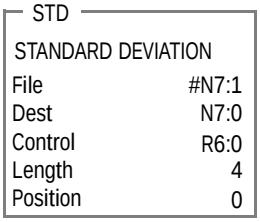
Instruction	Description
 Arc sine ASN	When input conditions go true, take the arc sine of the value in F8:17 and store the result in F8:18. Status Bit / Description C — always resets V — sets if overflow is generated; otherwise resets Z — sets if the result is zero; otherwise resets S — always resets
 Arc tangent ATN	When input conditions go true, take the arc tangent of the value in F8:21 and store the result in F8:22. Status Bit / Description C — always resets V — sets if overflow is generated; otherwise resets Z — sets if the result is zero; otherwise resets S — sets if the result is negative; otherwise resets
 Average AVE Status Bits: EN - Enable DN - Done bit ER - Error Bit	When the input conditions go from false-to-true, take the average of the file #N7:1 and store the result in N7:0. Status Bit / Description C — always resets V — sets if overflow is generated; otherwise resets Z — sets if the result is zero; otherwise resets S — sets if the result is negative; otherwise resets

Instruction	Description
 Clear CLR	When the input conditions are true, clear decimal file 9, word (set to zero). Status Bit: C — always reset; V — always reset; Z — always set; S — always reset
 Cosine COS	When input conditions go true, take the cosine of the value in F8:13 and store the result in F8:14. Status Bit: C — always resets; V — sets if overflow is generated; otherwise resets; Z — sets if the result is zero; otherwise resets; S — sets if the result is negative; otherwise resets

Instruction	Description
 Division DIV	When the input conditions are true, divide the value in Source A (N7:3) by the value in Source B (N7:4) and store the result in the Destination (N7:12). Status Bit: C — always resets; V — sets if division by zero or overflow; otherwise resets; Z — sets if the result is zero; otherwise resets; undefined if overflow is set; S — sets if the result is negative; otherwise resets; undefined if overflow is set

Instruction	Description
LN NATURAL LOG Source N7:0 5 Dest F8:20 1.609438 Natural log LN	When input conditions go true, take the natural log of the va in N7:0 and store the result in F8:20. Status Bit / Description C: always resets V: sets if overflow is generated; otherwise resets Z: sets if the result is zero; otherwise resets S: sets if the result is negative; otherwise resets
LOG LOG BASE 10 Source N7:2 5 Dest F8:3 0.6989700	When input conditions go true, take the log base 10 of the value in N7:2 and store the result in F8:3. Status Bit / Description C: always resets V: sets if overflow is generated; otherwise resets Z: sets if the result is zero; otherwise resets S: sets if the result is negative; otherwise resets
MUL MULTIPLY Source A N7:3 3 Source B N7:4 1 Dest N7:12 3 Multiply MUL	When the input conditions are true, multiply the value in Source A (N7:3) by the value in Source B (N7:4) store the result in the Destination (N7:12). Status Bit / Description C: always resets V: sets if overflow is generated; otherwise resets Z: sets if the result is zero; otherwise resets S: sets if the result is negative; otherwise resets

Instruction	Description
 Negate NEG	When the input conditions are true, take the opposite sign of the Source (N7:3) and store the result in the Destination (N7:12). This instruction turns positive values into negative values and negative values into positive values. Status Bit / Description: C — sets if the operation generates a carry; otherwise resets V — sets if overflow is generated; otherwise resets Z — sets if the result is zero; otherwise resets S — sets if the result is negative; otherwise resets
 Sine SIN	When input conditions go true, take the sine of the value in F8:11 and store the result in F8:12. Status Bit / Description: C — always resets V — sets if overflow is generated; otherwise resets Z — sets if the result is zero; otherwise resets S — sets if the result is negative; otherwise resets
 Square Root SQR	When the input conditions are true, take the square root of th Source (N7:3) and store the result in the Destination (N7:12). Status Bit / Description: C — always resets V — sets if overflow occurs during floating point to integer conversion; otherwise resets Z — sets if the result is zero; otherwise resets S — always reset

Instruction		Description
	Sort SRT Status Bits: EN-Enable DN-Done Bit ER-Error Bit	When the input conditions go from false-to-true, the values in N7:1, N7:2, N7:3.and N7:4 are sorted into ascending order.
	Standard Deviation STD Status Bits: EN - Enable DN - Done Bit ER - Error Bit	When the input conditions go from false-to-true, take the standard deviation of the values in file #N7:1 and store the result in the Destination (N7:0). Status Bit / Description C: always resets V: sets if overflow is generated; otherwise resets Z: sets if the result is zero; otherwise resets S: always resets

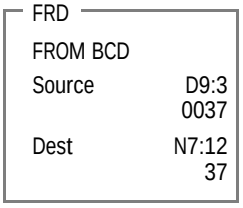
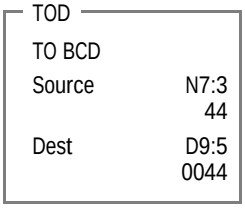
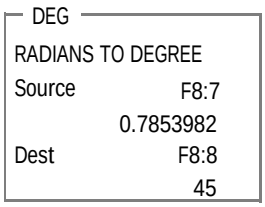
Instruction	Description
SUB SUBTRACT Source A N7:33 Source B N7:41 Dest N7:122 Subtract SUB	When the input conditions are true, subtract the value in Sour B (N7:4) from the value in Source A (N7:3) and store the result the Destination (N7:12). Status Bit: C — sets if borrow is generated; otherwise resets Status Bit: V — sets if underflow is generated; otherwise resets Status Bit: Z — sets if the result is zero; otherwise resets Status Bit: S — sets if the result is negative; otherwise resets
TAN TANGENT Source F8:15 0.7853982 Dest F8:16 1.000000 Tangent TAN	When input conditions go true, take the tangent of the value in F8:15 and store the result in F8:16. Status Bit: C — always resets Status Bit: V — sets if overflow is generated; otherwise resets Status Bit: Z — sets if the result is zero; otherwise resets Status Bit: S — sets if the result is negative; otherwise resets
XPY X TO POWER OF Y Source A N7:45 Source B N7:52 Dest N7:625 X to the power of Y XPY	When input conditions go true, take the the value in N7:4, raise it to the power stored in N7:5, and store the result in Status Bit: C — always resets Status Bit: V — sets if overflow is generated; otherwise resets Status Bit: Z — sets if the result is zero; otherwise resets Status Bit: S — sets if the result is negative; otherwise resets

Logical Instructions

Instruction		Description
AND BITWISE AND Source A D9:3 3F37 Source B D9:4 00FF Dest D9:5 0037	AND	When the input conditions are true, the controller performs ar AND operation (bit-by-bit) between Source A (D9:3) and Sourc B (D9:4) and stores the result in the Destination (D9:5). The truth table for an AND operation is: Source ASource BResult 000 100 010 111
NOT NOT Source A D9:3 00FF Dest D9:5 FF00	NOT Operation	When the input conditions are true, the controller performs a NOT (takes the opposite of) operation (bit-by-bit) on the Sourc (D9:3) and stores the result in the Destination (D9:5). The trut table for a NOT operation is: SourceDestination 01 10
OR BITWISE INCLUSIVE OR Source A D9:3 3F37 Source B D9:4 00FF Dest D9:5 3FFF	OR	When the input conditions are true, the controller performs ar OR operation (bit-by-bit) between Source A (D9:3) and Source (D9:4) and stores the result in the Destination (D9:5). The trut table for an OR operation is: Source ASource BResult 000 101 011 111
XOR BITWISE EXCLUSIVE OR Source A D9:3 3F37 Source B D9:4 3F37 Dest D9:5 0000	Exclusive OR XOR	When the input conditions are true, the controller performs ar exclusive OR operation (bit-by-bit) between Source A (D9:3) ar Source B (D9:4) and stores the result in the Destination (D9:5) The truth table for an XOR operation is: Source ASource BResult 000 101 011 110

Status Bit	Descriptio
C	always
V	always
Z	sets if the result is zero; otherwise
S	sets if the most significant bit (bit 15 for decimal or bit 17 for octal) is set (1); otherwise resets

Conversion Instructions

Instruction		Description
	Convert from BCD FRD	When the input conditions are true, convert the BCD value in the Source (D9:3) to a integer value and store the result in the Destination (N7:12). The source must be in the range of Status Bit / Description C: always resets V: always resets Z: sets if the destination value is zero; otherwise resets S: always resets
	Convert to BCD TOD	When the input conditions are true, convert the integer value in Source (N7:3) to a BCD format and store the result in the Status Bit / Description C: always resets V: sets if the source value is negative or greater than 9999 (i.e. outside of the range of 0-9999) Z: sets if the destinationvalue is zero; otherwise resets S: always resets
	Convert to Degrees DEG	When the input conditions are true, convert radians (the value in Source A) to degrees and stores the result in the Destination (Source times 180/p). Status Bit / Description C: always resets V: sets if overflow generated; otherwise resets Z: sets if result is zero; otherwise resets S: sets if result is negative; otherwise resets

Instruction		Description
RAD DEGREES TO RADIAN Source N7:9 45 Dest F8:10 0.785398	Convert to Radians RAD	When the input conditions are true, convert degrees (the value in Source A) to radians and stores the result in the Destination (Source times p/180). Status Bit: C — always resets V — sets if overflow generated; otherwise resets Z — sets if result is zero; otherwise resets S — sets if result is negative; otherwise resets

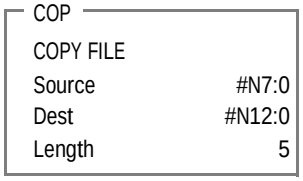
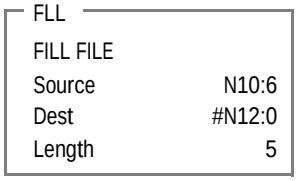
Bit Modify and Move Instructions

Instruction		Description
MOV MOVE Source N7:3 20 Dest F8:12 20.000000	Move MOV	When the input conditions are true, move a copy of the value ir Source (N7:3) to the Destination (F8:12), converting from one data type to another This overwrites the original value in the Destination. Status Bit: C — always resets V — sets if overflow is generated during floating point-to-integer conversion; otherwise resets Z — sets if the destination value is zero; otherwise resets S — sets if result MSB is set; otherwise resets
MVM MASKED MOVE Source D9:3 478F Mask D9:5 00FF Dest D9:12 008F	Masked Move MVM	When the input conditions are true, the controller passes the value in the Source (D9:3) through the Mask (D9:5) and stores t result in the Destination (D9:12). This overwrites the original value in the Destination. Status Bit: C — always resets V — always resets Z — sets if the result is zero; otherwise resets S — sets if most significant bit of resulting value is set; otherwise resets.

Instruction		Description
BTD BIT FIELD DISTRIB Source N7:3 0 Source bit 3 Dest N7:4 0 Dest bit 10 Length 6	Bit Distribute BTD	When the input conditions are true, the controller copies the number of bits specified by Length, starting with the Source bit (3) of the Source (N7:3), and placing the values in the Destination (N7:4), starting with the Destination bit (10).

File Instructions

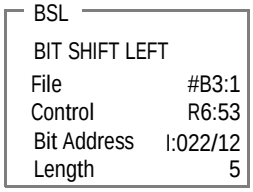
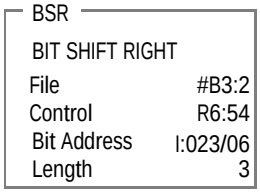
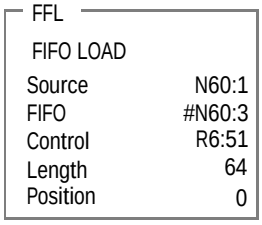
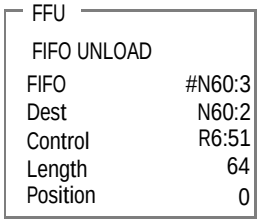
Instruction		Description
FAL FILE ARITH/LOGICAL Control R6:1 Length 8 Position 0 Mode ALL Dest #N15:10 Expression #N14:0 - 256	File Arithmetic and Logic FAL Status Bits: EN - Enable DN - Done Bit ER - Error Bit	When the input conditions go from false-to-true, the controller reads 8 elements of N14:0, and subtracts 256 (a constant) from each element. This example shows the result being stored in the eight elements beginning with N15:10. The control element R6:1 controls the operation. The Mode determines whether the controller performs the expression on all elements in the files (ALL) per program scan, one element in the files (INC) per false-to-true transition, or a specific number of elements (NUM) per scan. The FAL instruction can perform these operations: add (+), subtract (-), multiply (*), divide (|), convert from BCD (FRD), convert to BCD (TOD), square root (SQR), logical and (AND), logical or (OR), logical not (NOT), exclusive or (XOR), negate (-), clear (0), move, and the new math instructions (see the CPT list).
FSC FILE SEARCH/COMPARE Control R9:0 Length 90 Position 0 Mode 10 Expression #B4:0 <> #B5:0	File Search and Compare FSC Status Bits: EN - Enable DN - Done Bit ER - Error Bit IN - Inhibit Bit FD - Found Bit	When the input conditions go from false-to-true, the controller performs the not-equal-to comparison on 10 elements between files B4:0 and B5:0. Mode determines whether the controller performs the expression on all elements in the files (ALL) per program scan, one element in the files (INC) per false-to-true transition, or a specific number of elements (NUM) per scan. Control element R9:0 controls the operation. When the corresponding source elements are not equal (element B4:4 and B5:4 in this example), the controller stops the search and sets the found .FD and inhibit .IN bits so your ladder program can take appropriate action. To continue the search comparison, you must reset the .IN bit. To see a list of the available comparisons, see the comparisons listed under the CMP instruction.

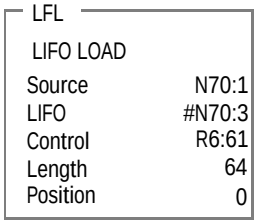
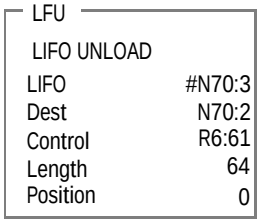
Instruction		Description
	File Copy COP	When the input conditions are true, the controller copies the contents of the Source file (N7) into the Destination file (N12). The source remains unchanged. The COP instruction copies the number of elements from the source as specified by the Length. As opposed to the MOV instruction, there is no data type conversion for this instruction.
	File Fill FLL	When the input conditions are true, the controller copies the value in Source (N10:6) to the elements in the Destination (N12). The FLL instruction only fills as many elements in the destination as specified in the Length. As opposed to the MOV instruction, there is no data type conversion for this instruction.

Diagnostic Instructions

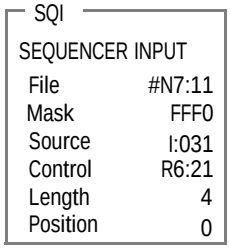
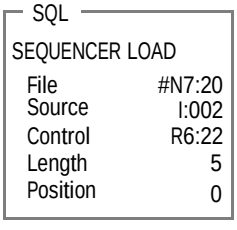
Instruction		Description
FBC FILE BIT COMPARE Source #I:031 Reference #B3:1 Result #N7:0 Cmp Control R6:4 Length 48 Position 0 Result Control R6:5 Length 10 Position 0	File Bit Compare FBC Status Bits: EN - Enable DN - Done Bit ER - Error Bit IN - Inhibit Bit FD - Found Bit	When the input conditions go from false-to-true, the controller compares the number of bits specified in the CMP Control Length (48) of the Source file (#I:031) with the bits in the Reference file (#B3:1). The controller stores the results (mismatched bit numbers) in the Result file (#N7:0). File R6:4 controls the compare and file R6:5 controls the file that contains the results. The file containing the results can hold up to 10 (the number specified in the Length field) mismatches between the compared files. ***Note:*** To avoid encountering a possible run-time error when executing this instruction, add a ladder rung that clears S:24 (indexed addressing offset) immediately before a FBC instruction.
DDT DIAGNOSTIC DETECT Source #I:030 Reference #B3:1 Result #N10:0 Cmp Control R6:0 Length 20 Position 0 Result Control R6:1 Length 5 Position 0	Diagnostic Detect DDT Status Bits: EN - Enable DN - Done Bit ER - Error Bit IN - Inhibit Bit FD - Found Bit	When the input conditions go from false-to-true, the controller compares the number of bits specified in the CMP Control Length (20) of the Source file (# I:030) with the bits in the Reference file (#B3:1). The controller stores the results (mismatched bit numbers) in the Result file (#N10:0). Control element R6:0 controls the compare and the control element R6:1 controls the file that contains the results (#N10:0). The file containing the results can hold up to 5 (the number specified in the Length field) mismatches between the compared files. The controller copies the source bits to the reference file for the next comparison. The difference between the DDT and FBC instruction is that each time the DDT instruction finds a mismatch, the controller changes the reference bit to match the source bit. You can use the DDT instruction to update your reference file to reflect changing machine or process conditions. ***Note:*** To avoid encountering a possible run-time error when executing this instruction, add a ladder rung that clears S:24 (indexed addressing offset) immediately before a DDT instruction.
DTR DATA TRANSITION Source I:002 Mask 0FFF Reference N63:11	Data Transition DTR	The DTR instruction compares the bits in the Source (I:002) through a Mask (0FFF) with the bits in the Reference (N63:11). When the masked source is different than the reference, the instruction is true for only 1 scan. The source bits are written into the reference address for the next comparison. When the masked source and the reference are the same, the instruction remains false.

Shift Register Instructions

Instruction		Description
	Bit Shift Left BSL Status Bits: EN - Enable DN - Done Bit ER - Error Bit UL - Unload Bit	If the input conditions go from false-to-true, the BSL instruction shifts the number of bits specified by Length (5) in File (B3), starting at bit 16 (B3:1/0 = B3/16), to the left by one bit position. The source bit (I:022/12) shifts into the first bit position, B3:1/0 (B3/16). The fifth bit, B3:1/4 (B3/20), is shifted into the UL bit of the control structure (R6:53).
	Bit Shift Right BSR Status Bits: EN - Enable DN - Done Bit ER - Error Bit UL - Unload Bit	If the input conditions go from false-to-true, the BSR instruction shifts the number of bits specified by Length (3) in File (B3), starting with B3:2/0 (=B3/32), to the right by one bit position. The source bit (I:023/06) shifts into the third bit position B3/34. The first bit (B3/32) is shifted into the UL bit of the control element (R6:54).
	FIFO Load FFL Status Bits: EN - Enable Load DN - Done Bit EM - Empty Bit	When the input conditions go from false-to-true, the controller loads N60:1 into the next available element in the FIFO file, #N60:3, as pointed to by R6:51. Each time the rung goes from false-to-true, the controller loads another element. When the FIFO file (stack) is full, (64 words loaded), the DN bit is set. See page F-8 for a description of prescan activities for this instruction.
	FIFO Unload FFU Status Bits: EU - Enable Unload DN - Done Bit EM - Empty Bit	When the input conditions go from false-to-true, the controller unloads an element from #N60:3 into N60:2. Each time the rung goes from false-to-true, the controller unloads another value. All the data in file #N60:3 is shifted one position toward N60:3. When the file is empty, the EM bit is set. See page F-8 for a description of prescan activities for this instruction.

Instruction		Description
	LIFO Load LFL Status Bits: EN - Enable Load DN - Done Bit EM - Empty Bit	When the input conditions go from false-to-true, the controller loads N70:1 into the next available element in the LIFO file #N70:3, as pointed to by R6:61. Each time the rung goes from false-to-true, the controller loads another element. When the LIFO file (stack) is full (64 words have been loaded), the DN bit is set. See page F-8 for a description of prescan activities for this instruction.
	LIFO Unload LFU Status Bits: EU - Enable Unload DN - Done Bit EM - Empty Bit	When the input conditions go from false-to-true, the controller unloads the last element from #N70:3 and puts it into N70:2. Each time the rung goes from false-to-true, the controller unloads another element. When the LIFO file is empty, the EM bit is set. See page F-8 for a description of prescan activities for this instruction.

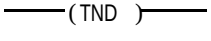
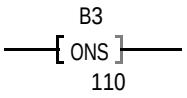
Sequencer Instructions

Instruction		Description
	Sequencer Input SQI	The SQI instruction filters the Source (I:031) input image data through a Mask (FFF0) and compare the result to Reference data (#N7:11) to see if the two values are equal. The operation is controlled by the information in the control file R6:21. When the status of all unmasked bits of the word pointed to by control element R6:21 matches the corresponding reference bits, the rung condition remains true if preceded by a true rung condition.
	Sequencer Load SQL Status Bits: EN - Enable DN - Done Bit ER - Error Bit	The SQL instruction loads data into the sequencer File (#N7:20) from the source word (I:002) by stepping through the number of elements specified by Length (5) of the Source (I:002), starting at the Position (0). The operation is controlled by the information in the control file R6:22. When the rung goes from false-to-true, the SQL instruction increments the next step in the sequencer file and loads the data into it for every scan that the rung remains true. See page F-8 for a description of prescan operation for this instruction.

Instruction		Description
SQO SEQUENCER OUTPUT File #N7:1 # Mask 0F0F Dest O:014 Control R6:20 Length 4 Position 0	Sequencer Output SQO Status Bits: EN - Enable DN - Done Bit ER - Error Bit	When the rung goes from false-to-true, the SQO instruction increments to the next step in the sequencer File (#N7:1). The data in the sequencer file is transferred through a Mask (0F0F) to the Destination (O:014) for every scan that the rung remains true. See page F-8 for a description of prescan operation for this instruction.

Program Control Instructions

Instruction		Description
(MCR)	Master Control Reset MCR	If the input conditions are true, the program scans the rungs between MCR instruction rungs and processes the outputs normally. If the input condition is false, rungs between the MCR-instruction rungs are executed as false.
10 (JMP)	Jump JMP	If the input conditions are true, the controller skips rungs by jumping to the rung identified by the label (10).
10 [LBL]	Label LBL	When the controller reads a JMP instruction that corresponds to label 10, the controller jumps to the rung containing the label and starts executing. **Important:** Must be the first instruction on a rung.
FOR FOR Label Number 0 Index N7:0 Initial Value 0 Terminal Value 10 Step Size 1	FOR Loop FOR	The controller executes the rungs between the FOR and the NXT instruction repeatedly in one program scan, until it reaches the terminal value (10) or until a BRK instruction aborts the operation. Step size is how the loop index is incremented. See page F-8 for a description of prescan operation for this instruction.
NXT NEXT Label Number 0	Next NXT	The NXT instruction returns the controller to the corresponding FOR instruction, identified by the label number specified in the FOR instruction. NXT must be programmed on an unconditional rung that is the last rung to be repeated in a For-Next loop.
[BRK]	Break BRK	When the input conditions go true, the BRK instruction aborts a For-Next loop.

Instruction		Description
JSR JUMP TO SUBROUTINE Program File 90 Input par N16:23 Input par N16:24 Input par 231 Return par N19:11 Return par N19:12	Jump to Subroutine JSR	If the input conditions are true, the controller starts running a subroutine Program File (90). The controller passes the Input Parameters (N16:23, N16:24, 231) to the subroutine and the RET instruction passes Return Parameters (N19:11, N19:12) back to the main program, where the controller encountered the JSR instruction.
SBR SUBROUTINE Input par N43:0 Input par N43:1 Input par N43:2	Subroutine SBR	The SBR instruction is the first instruction in a subroutine file. This instruction identifies Input Parameters (N43:0, N43:1, N43:2) the controller receives from the corresponding JSR instruction. You do not need the SBR instruction if you do not pass input parameters to the subroutine.
RET RETURN ( ) Return par N43:3 Return par N43:4	Return RET	If the input conditions are true, the RET instruction ends the subroutine and stores the Return Parameters (N43:3, N43:4) to be returned to the JSR instruction in the main program.
	Always False AFI	The AFI instruction disables the rung (i.e., the rung is always false).
	Temporary End TND	If the input conditions are true, the TND instruction stops the controller from scanning the rest of the program (i.e., this instruction temporarily ends the program).
	One Shot ONS	If the input conditions preceding the ONS instructions on the same rung go from false-to-true, the ONS instruction conditions the rung so that the output is true for one scan. The rung is false on successive scans. See page F-8 for a description of prescan operation for this instruction.
OSF ONE SHOT FALLING Storage Bit B3/0 Output Bit 15 Output Word N7:0	One Shot Falling OSF Status Bits: OB - Output Bit SB - Storage Bit	The OSF instruction triggers an event to occur one time. Use the OSF instruction whenever an event must start based on the change of state of a rung from true-to-false, not on the resulting rung status. The output bit (N7:0/15) is set (1) for one program scan when the rung goes from true-to-false. See page F-8 for a description of prescan operation for this instruction.
OSR ONE SHOT RISING Storage Bit B3/0 Output Bit 15 Output Word N7:0	One Shot Rising OSR Status Bits: OB - Output Bit SB - Storage Bit	The OSR instruction triggers an event to occur one time. Use the OSR instruction whenever an event must start based on the change of state of a rung from false-to-true, not on the resulting rung status. The output bit (N7:0/15) is set (1) for one program scan when the rung goes from false-to-true. See page F-8 for a description of prescan operation for this instruction.

Instruction		Description
	SFC Reset SFR	The SFR instruction resets the logic in a sequential function chart. When the SFR instruction goes true, the controller performs a lastscan/postscan on all active steps and actions in the selected file, and then resets the logic in the SFC on the next program scan. The chart remains in this reset state until the SFR instruction goes false.
	End of Transition EOT	The EOT instruction should be the last instruction in a transition file. If you do not use an EOT instruction, the controller always evaluates the transition as true. See page F-8 for a description of prescan operation for this instruction.
	User Interrupt Disable UID	The UID instruction temporarily disables an interrupt-driven ladder program (such as an STI or PII) from interrupting the currently executing program.
	User Interrupt Enable UIE	The UIE instruction re-enables the interrupt-driven ladder program to interrupt the currently executing ladder program.

Process Control, Message Instructions

Instruction		Description
PID PID Control Block PD10:0 Proc Variable N15:13 Tieback N15:14 Control Output N20:21	Proportional, Integral, and Derivative PID Status Bits: EN - Enable DN - Done Bit (for N control blocks only)	The control block (PD10:0) contains the instruction information for the PID. The PID gets the process variable from N15:13 and sends the PID output to N20:21. The tieback stored in N15:14 handles the manual control station. If you use an N control block, the rung must transition from false to true for execution. If you use PD control block, then there is no done bit. Also, the rung input conditions need to be true. See page F-8 for a description of prescan operation for this instruction.
MSG SEND/RECEIVE MESSAGE Control Block MG7:10 Bit # Status Bits 15 EN - Enable 14 ST - Start Bit 13 DN - Done Bit 12 ER - Error Bit 11 CO - Continuous 10 EW - Enabled-Waiting 9 NR - No Response		If the input conditions go from false to true, the data is transferred according to the instruction parameters you set when you entered the message instruction. The Control Block (MG7:10) contains status and instruction parameters. You can also use N control blocks. For continuous MSGs, condition the rung to be true for only one scan. See page F-8 for a description of prescan operation for this instruction.

Block Transfer Instructions

Integer (N) control block

Word Offset	Description
0	status bits (see below)
1	requested word count
2	transmitted word count
3	file number
4	element number

Block Transfer (BT) control block

Word Mnemonic	Description
.EN through .RW	status bits
.RLEN	requested length
.DLEN	transmitted word length/error code
.FILE	file number
.ELEM	element number
.RGS	rack/group/slot

Word 0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
EN	ST	DN	ER	CO	EW	NR	TO	RW	**	rack	**	**	group**		slot	

Instruction		Description
BTR BLOCK TRANSFER READ Rack 1 Group 0 Module 0 Control Block BT11:100 Data File N10:110 Length 40 Continuous Y	Block Transfer Read BTR	If the input conditions go from false to true, a block transfer read is initiated for the I/O module located at rack 1, group 0, module 0. The Control Block (BT11:100, 6-word file) contains status for the transfer. The Data File (N10:110) is where the data read from the module is stored. The BT Length (40) identifies the number of words in the transfer. A non-continuous block transfer is queued and run only once on a false-to-true rung transition; a continuous block transfer is repeatedly requeued. You can also use the N data type for the control blocks. See page F-8 for a description of prescan operation for this instruction.

PLC-5/30, -5/40, -5/40E, -5/40L -5/60, -5/60L, -5/80, -5/80E controllers		PLC-5/40, -5/40L, -5/60, -5/60L, -5/80, -5/40E, -5/80E controllers		PLC-5/60, -5/60L, -5/80, -5/80E controllers	
S:7 bit #	BT queue full for rack	S:32 bit #	BT queue full for rack	S:34 bit #	BT queue full for rack
08(1)	0	08	10	08	20
09[1]	1	09	11	09	21
10[1]	2	10	12	10	22
11[1]	3	11	13	11	23
12	4	12	14	12	24
13	5	13	15	13	25
14	6	14	16	14	26
15	7	15	17	15	27

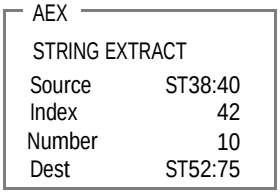
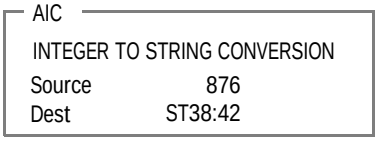
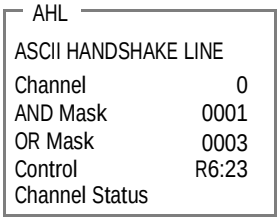
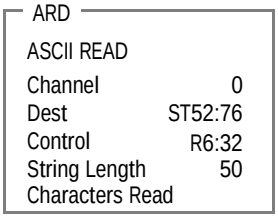
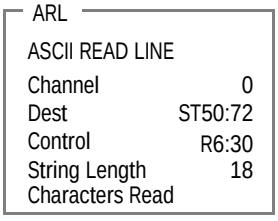
(1) PLC-5/11, -5/20, and 5/20E controllers also

Instruction		Description
BTW BLOCK TRANSFER WRITE Rack 1 Group 0 Module 0 Control Block BT11:0 Data File N10:10 Length 40 Continuous Y	Block Transfer Write BTW	If the input conditions go from false-to-true, the block transfer write is initiated for the I/O module located at rack 1, group 0, module 0. The Control Block (BT11:0, 6-word file) contains status for the transfer. The Data File contains the data to write to the module (N10:10). The BT Length (40) identifies the number of words in the transfer. A non-continuous block transfer is queued and run only once on a false-to-true rung transition; a continuous block transfer is repeatedly requeued. You can also use the N data type for the control block. See page f-8 for a description of prescan operation for this instruction.

ASCII Instructions

Status Bits:
EN - EnableEM - Empty Bit
DN - Done BitEU - Queue
ER - Error BitFD - Found Bit

Instruction		Description
ABL ASCII TEST FOR LINE Channel 0 Control R6:32 Characters	ASCII Test for Line ABL	If input conditions go from false-to-true, the controller reports the number of characters in the buffer, up to and including the end-of-line characters and puts this value into the position word of the control structure (R6:32.POS). The controller also displays this value in the characters field of the display. See page F-8 for a description of prescan operation for this instruction.
ACB ASCII CHARS IN BUFFER Channel 0 Control R6:32 Characters	ASCII Characters in Buffer ACB	If input conditions go from false-to-true, the controller reports the total number of characters in the buffer and puts this value into the position word (.POS) of the control structure. The controller also displays this value in the characters field of the display. See page F-8 for a description of prescan operation for this instruction.
ACI STRING TO INTEGER CONVERSION Source ST38:90 Dest N7:123 75	Convert ASCII String to Integer ACI	If input conditions are true, the controller converts the string in ST38:90 to an integer and stores the result in N7:123. Status Bit / Description C: set if a carry was generated during the conversion; otherwise resets V: set if source is > 32,767 or < -32,768, otherwise resets Z: set if source is zero; otherwise resets S: set if destination is negative; otherwise resets
ACN STRING CONCATENATE Source A ST38:90 Source B ST37:91 Dest ST52:76	ASCII String Concatenate ACN	If input conditions are true, the controller concatenates the string in ST38:90 with the string in ST37:91 and store the result in ST52:76.

Instruction		Description
	ASCII String Extract AEX	If input conditions are true, the controller extracts 10 characters starting at the 42nd character of ST38:40 and store the result in ST52:75.
	Convert Integer to ASCII String AIC	If input conditions are true, the controller converts the value 876 to a string and store the result in ST38:42.
	ASCII Handshake Lines AHL Status Bits: EN-Enable DN-Done Bit ER-Error Bit	If input conditions go from false-to-true, the controller uses the AND and OR masks to determine whether to set or reset the DTR (bit 0) and RTS (bit 1) lines, or leave them unchanged. Bit 0 and 1 of the AND mask cause the line(s) to reset if 1 and leave the line(s) unchanged if 0. BIt 0 and 1 of the OR mask cause the line(s) to set if 1 and leave the line(s) unchanged if 0. See page F-8 for a description of prescan operation for this instruction.
	ASCII Read ARD Status Bits EN - Enable DN - Done Bit ER - Error Bit UL - Unload EM - Empty EU - Queue	If input conditions go from false-to-true, read 50 characters from the buffer and move them to ST52:76. The number of characters read is stored in R6:32.POS and displayed in the Characters Read Field of the instruction display. See page F-8 for a description of prescan operation for this instruction.
	ASCII Read Line ARL Status Bits EN - Enable DN - Done Bit ER - Error Bit UL - Unload EM - Empty EU - Queue	If input conditions go from false-to-true, read 18 characters (or until end-of-line) from the buffer and move them to ST50:72. The number of characters read is stored in R6:30.POS and displayed in the Characters Read Field of the instruction display. See page F-8 for a description of prescan operation for this instruction.

Instruction		Description
ASC STRING SEARCH Source ST38:40 Index 35 Search ST52:80 Result 42	ASCII String Search ASC	If input conditions are true, search ST52:80 starting at the 35th character, for the string found in ST38:40. In this example, the string was found at index 42. If the string is not found, the ASCII instruction minor fault bit S:17/8 is set and the result is zero.
ASR ASCII STRING COMPARE Source A ST37:42 Source B ST38:90	ASCII String Compare ASR	If the string in ST37:42 is identical to the string in ST38:90, the instruction is true. Note that this is an input instruction. An invalid string length causes the ASCII instruction error minor fault bit S:17/8 to be set, and the instruction is false.
AWA ASCII WRITE APPEND Channel 0 Source ST52:76 Control R6:32 String Length 50 Characters Sent	ASCII Write Append AWA Status Bits EN - Enable DN - Done Bit ER - Error Bit UL - Unload EM - Empty EU - Queue	If input conditions go from false-to-true, read 50 characters from ST52:76 and write it to channel 0 and append the two character configuration in the channel configuration (default CR/LF). The number of characters sent is stored in R6:32.POS and displayed in the characters sent field of the instruction display. See page F-8 for a description of prescan operation for this instruction.
AWT ASCII WRITE Channel 0 Source ST37:40 Control R6:23 String Length 40 Characters Sent	ASCII Write AWT Status Bits EN - Enable DN - Done Bit ER - Error Bit UL - Unload EM - Empty EU - Queue	If input conditions go from false-to-true, write 40 characters from ST37:40 to channel 0. The number of characters sent is stored in R6:23.POS and displayed in the characters sent field of the instruction display. See page F-8 for a description of prescan operation for this instruction.

Bit and Word Instructions

Category	Code	Title	Execution Time (µs) Integer		Execution Time (µs) Floating Point		Words of Memory (1)
			True	False	True	False	
Relay	XIC	examine if closed	.32	.16			1(2)
	XIO	examine if open	.32	.16			1[2]
	OTL	output latch	.48	.16			1[2]
	OTU	output unlatch	.48	.16			1[2]
	OTE	output energize	.48	.48			1[2]
Branch		branch end	.16	.16			1
		next branch					1
		branch start					1
Timer and Counter	TON	timer on(0.01 base) (1.0 base)	3.8 4.1	2.6 2.5			2-3
	TOF	timer off(0.01 base) (1.0 base)	2.6 2.6	3.2 3.2			2-3
	RTO	retentive timer on (0.01 base) (1.0 base)	3.8 4.1	2.4 2.3			2-3
	CTU	count up	3.4	3.4			2-3
	CTD	count down	3.3	3.4			2-3
	RES	reset	2.2	1.0			2-3

(1) Use the larger number for addresses beyond 2048 words in the controller's data table.

(2) For every bit address above the first 256 words of memory in the data table, add 0.16 µs and 1 word of memory.

Category	Code	Title	Execution Time (µs) Integer		Execution Time (µs) Floating Point		Words of Memory (1)
			True	False	True	False	
Arithmetic	ADD	add	6.1	1.4	14.9	1.4	4-7
	SUB	subtract	6.2	1.4	15.6	1.4	4-7
	MUL	multiply	9.9	1.4	18.2	1.4	4-7
	DIV	divides	12.2	1.4	23.4	1.4	4-7
	SQR	square root	9.9	1.3	35.6	1.3	3-5
	NEG	negate	4.8	1.3	6.0	1.3	3-5
	CLR	clear	3.4	1.1	3.9	1.1	2-3
	AVE	average file	152+E25.8	30	162+E22.9	36	4-7
	STD	standard deviation	262+E92.5	34	295+E85.5	34	4-7
	TOD	convert to BCD	7.8	1.3			3-5
	FRD	convert from BCD	8.1	1.3			3-5
	RAD	radian	57.4	1.4	50.1	1.4	3-5
	DEG	degree	55.9	1.4	50.7	1.4	3-5
	SIN	sine			414	1.4	3-5
	COS	cosine			404	1.4	3-5
	TAN	tangent			504	1.4	3-5
	ASN	inverse sine			426	1.4	3-5
	ACS	inverse cosine			436	1.4	3-5
	ATN	inverse tangent			375	1.4	3-5
	LN	natural log	409	1.4	403	1.4	3-5
	LOG	log	411	1.4	403	1.4	3-5
	XPY	X to the power of Y	897	1.5	897	1.5	4-7
	SRT	sort file					3-5
		(5/11, -5/20)	276 + 12[E**1.34]	227	278 + 16[E**1.35]	227	
		(-5/30, -5/40, -5/60, -5/80)	224 + 25[E**1.34]	189	230 + 33[E**1.35]	189	

(1) Use the larger number for addresses beyond 2048 words in the controller's data table.

E = number of elements acted on per scan

SRT true is only an approximation. Actual time depends on the randomness of the numbers.

File, Program Control, and ASCII Instructions

Category	Code	Title	Time (µs) Integer		Time (µs) Floating Point		Words of Memory[1]
			True	False	True	False	
File Arithmetic and Logic	FAL	all	11 + (S[2.3 + i])E	6.16 + Wi[0.16]	11 + (Σ[2.3 + i])E	6.16 + Wi[0.16]	3-5 +Wi
File Search and Compare	FSC	all	11 + (S[2.3 + i])E	6.16 + Wi[0.16]	11 + (Σ[2.3 + i])E	6.16 + Wi[0.16]	3-5 +Wi
File	COP	copy	16.2+E[0.72]	1.4	17.8+E[1.44]	1.4	4-6
		counter, timer, and control	15.7+E[2.16]	1.4			
	FLL	fill	15.7+E[0.64]	1.5	18.1+E[0.80]	1.5	4-6
		counter, timer, and control	15.1+E[1.60]	1.5			
Shift Register	BSL	bit shift left	10.6+B[0.025]	5.2			4-7
	BSR	bit shift right	11.1 + B[0.025]	5.2			4-7
	FFL	FIFO load	8.9	3.8			4-7
	FFU	FIFO unload	10.0+E[0.43]	3.8			4-7
	LFL	LIFO load	9.1	3.7			4-7
	LFU	LIFO unload	10.6	3.8			4-7
Diagnostic	FBC	0 mismatch	15.4 + B[0.055]	2.9			6-11
		1 mismatch	22.4 + B[0.055]	2.9			
		2 mismatches	29.9+ B[0.055]	2.9			
	DDT	0 mismatch	15.4 + B[0.055]	2.9			6-11
		1 mismatch	24.5 + B[0.055]	2.9			
		2 mismatches	34.2 + B[0.055]	2.9			
	DTR	data transitional	5.3	5.3			4-7

(1) Use the larger number for addresses beyond 2048 words in the controller's data table.

i = execution time of each instruction (e.g., ADD, SUB, etc.) used within the FAL or the FSC expression

E = number of elements acted on per scan

B = number of bits acted on per scan

Wi = number of words used by the instruction (e.g., ADD, SUB, etc.) within the FAL or FSC expression

FAL or FSC instructions are calculated with short direct addressing

Category	Code	Title	Time (μs) Integer		Time (μs) Floating Point		Words of Memory[1]
			True	False	True	False	
Sequencer	SQI	sequencer input	7.9	1.3			5-9
	SQL	sequencer load	7.9	3.5			4-7
	SQO	sequencer output	9.7	3.7			5-9
Immediate I/O[2]	IIN	immediate input • PLC-5/11, -5/20, and -5/20E • PLC5/30, -5/40, -5/40E, -5/40L -5/60, -5/60L, and -5/80, -5/80E	• 357 • 307	1.1			2
	IOT	immediate output • PLC-5/11, -5/20, and -5/20E • PLC5/30, -5/40, -5/40E, -5/40L -5/60, -5/60L, -5/80, and -5/80E	• 361 • 301	1.1			2
Zone Control	MCR	master control	0.16	0.16			1
Program Control	JMP	jump	8.9+(file# - 2) * 0.96	1.4			2
	JSR[3] /RET	jump to subroutine /return					3+parameters/JSR
		— 0 parameters	12.3	1.0	not applicable	not applicable	1+parameters/RET
		— 1 parameter	16.1	1.0	17.3	1.0	
		— increase/ parameter	3.8	not applicable	5.0	not applicable	
	SBR						1+ parameters

(1) Use the larger number for addresses beyond 2048 words in the controller's data table.

(2) Timing for immediate I/O instructions is the time for the instruction to queue-up for processing.

(3) Calculate execution times as follows: (time) + (quantity of additional parameters)(time/parameter). For example: if you are passing 3 integer parameters in a JSR within a PLC-5/11 controller, the execution time = 16.1 + (2)(3.8) = 23.7 ms

Category	Code	Title	Time (µs) Integer		Time (µs) Floating Point		Words of Memory(1)
			True	False	True	False	
Program Control	LBL	label	0.16	0.16			2
	END	end	negligible				1
	TND	temporary end					1
	EOT	end of transition					1
	AFI	always false	0.16	0.16			1
	ONS	one shot	3.0	3.0			2-3
	OSR	one shot rising	6.2	6.0			4-6
	OSF	one shot falling	6.2	5.8			4-6
	FOR/ NXT	for next loop	8.1+ L[15.9]+ (file# - 2) * 0.96	5.3 + N[0.75]			FOR 5-9 NXT 2
	BRK	break	11.3 + N[0.75]	0.9			1
	UID	user interrupt disable (PLC-5/11, -5/20, -5/30, -5/40, -5/60, and -5/80 controllers)	175 119	1.0			1
	UIE	user interrupt enable (PLC-5/11, -5/20, -5/30, -5/40, -5/60, and -5/80 controllers)	170 100	1.0			1

(1) Use the larger number for addresses beyond 2048 words in the controller's data table.

L = number of FOR/NXT loops

N = number of words in memory between FOR/NXT or BRK/NXT

Category	Code	Title	Time (µs) Integer		Time (µs) Floating Point		Words of Memory(1)
			True	False	True	False	
Process Control	PID	PID loop control					5-9
Gains		Independent • PLC-5/11, -5/20, -5/20E • PLC-5/30, -5/40, -5/40E, -5/40L -5/60, -5/60L -5/80, -5/80E	• 462 • 655	3.0	1120	58	
		ISA • PLC-5/11, -5/20, and -5/20E • PLC-5/30, -5/40, -5/40E, -5/40L -5/60, -5/60L, -5/80, and -5/80E	• 560 • 895		1180		
Modes		Manual • PLC-5/11, -5/20, and -5/20E • PLC-5/30, -5/40, -5/40E, -5/40L -5/60, -5/60L, -5/80, and -5/80E	• 372 • 420		1150		
		Set Output • PLC-5/11, -5/20, and -5/20E • PLC-5/30, -5/40, -5/40E, -5/40L -5/60, -5/60L, -5/80, and -5/80E	• 380 • 440		1130		
Cascade		Slave			1530		
		Master			1080		
ASCII (2)	ABL	test buffer for line • PLC-5/11, -5/20, and -5/20E • PLC-5/30, -5/40, -5/40E, -5/40L -5/60, -5/60L, -5/80, and -5/80E	• 316 • 388	• 214 • 150			3-5

(1) Use the larger number for addresses beyond 2048 words in the controller's data table.

(2) Timing for ASCII instructions is the time for the instruction to queue-up for processing in channel 0.

C = number of ASCII characters

Category	Code	Title	Time (µs) Integer		Time (µs) Floating Point		Words of Memory[1]
			True	False	True	False	
	ACB	no. of characters in buffer • PLC-5/11, -5/20, and -5/20E • PLC-5/30, -5/40, -5/40E, -5/40L -5/60, -5/60L, -5/80, and -5/80E	• 316 • 389	• 214 • 150			3-5
	ACI	string to integer • PLC-5/11, -5/20, and -5/20E • PLC-5/30, -5/40, -5/40E, -5/40L -5/60, -5/60L, -5/80, and -5/80E	• 220 + C[11] • 140 + C[21.4]	1.4			3-5
	ACN	string concatenate • PLC-5/11, -5/20, and -5/20E • PLC-5/30, -5/40, -5/40E, -5/40L -5/60, -5/60L, -5/80, and -5/80E	• 237 + C[2.6] • 179 + C[5.5]	1.9			4-7
	AEX	string extract • PLC-5/11, -5/20, and -5/20E • PLC-5/30, -5/40, -5/40E, -5/40L -5/60, -5/60L, -5/80, and -5/80E	• 226 + C[1.1] • 159 + C[2.2]	1.9			5-9
	AHL¡	set or reset lines • PLC-5/11, -5/20, and -5/20E • PLC-5/30, -5/40, -5/40E, -5/40L -5/60, -5/60L, -5/80, and -5/80E	• 318 • 526	• 213 • 157			5-9

(1) Use the larger number for addresses beyond 2048 words in the controller's data table.

Category	Code	Title	Time (µs) Integer		Time (µs) Floating Point		Words of Memory[1]
			True	False	True	False	
ASCII[2]	AIC	integer to string • PLC-5/11, -5/20, and -5/20E • PLC-5/30, -5/40, -5/40E, -5/40L -5/60, -5/60L, -5/80, and -5/80E	• 260 • 270	1.4			3-5
	ARD	read characters • PLC-5/11, -5/20, and -5/20E • PLC-5/30, -5/40, -5/40E, -5/40L -5/60, -5/60L, -5/80, and -5/80E	• 315 • 380	• 214 • 149			4-7
	ARL	read line • PLC-5/11, -5/20, and -5/20E • PLC-5/30, -5/40, -5/40E, -5/40L -5/60, -5/60L, -5/80, and -5/80E	• 316 • 388	• 214 • 151			4-7
	ASC	string search • PLC-5/11, -5/20, and -5/20E • PLC-5/30, -5/40, -5/40E, -5/40L -5/60, -5/60L, -5/80, and -5/80E	• 222 + C[1.7] • 151 + C[3.0]	1.9			5-9
	ASR	string compare • PLC-5/11, -5/20, and -5/20E • PLC-5/30, -5/40, -5/40E, -5/40L -5/60, -5/60L, -5/80, and -5/80E	• 234 + C[1.3] • 169 + C[2.4]	• 202 • 119			3-5

(1) Use the larger number for addresses beyond 2048 words in the controller's data table.

(2) Timing for ASCII instructions is the time for the instruction to queue-up for processing in channel 0.

C = number of ASCII characters

Category	Code	Title	Time (µs) Integer		Time (µs) Floating Point		Words of Memory[1]
			True	False	True	False	
ASCII[2]	AWA	write with append • PLC-5/11, -5/20, and -5/20E • PLC-5/30, -5/40, -5/40E, -5/40L -5/60, -5/60L, -5/80, and -5/80E	• 319 • 345	• 215 • 154			4-7
	AWT	write • PLC-5/11, -5/20, and -5/20E • PLC-5/30, -5/40, -5/40E, -5/40L -5/60, -5/60L, -5/80, and -5/80E	• 318 • 344	• 215 • 151			4-7

(1) Use the larger number for addresses beyond 2048 words in the controller's data table.

(2) Timing for ASCII instructions is the time for the instruction to queue-up for processing in channel 0.

C = number of ASCII characters

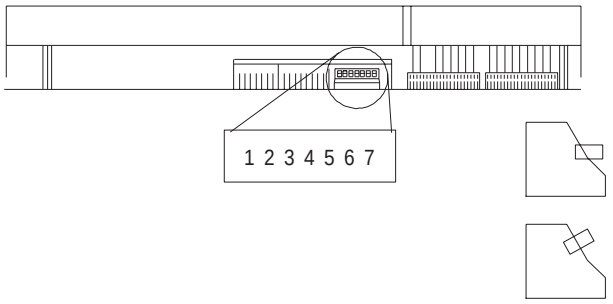
Switch Setting Reference

Using This Chapter

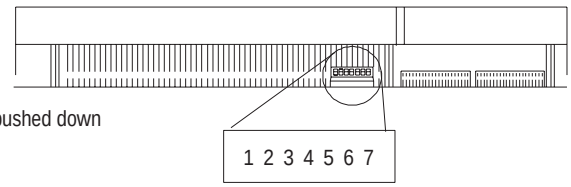
Controller Switches

Switch 1

Side View of PLC-5/11, -5/20, -5/26, -5/20E controllers Switch Assembly SW1



Side View of PLC-5/30, -5/40, -5/46, -5/40L, -5/60, -5/60L, -5/80, -5/86, -5/40E, and -5/80E controllers Switch Assembly SW1



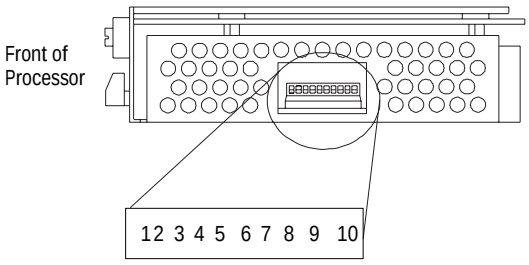
To Select DH+ Baud Rate for Channel 1A:	Set sSitch:	To:
DH+ address	1 through 6	(See below)
DH+ baud rate	7	on (down)57.6 kbps off (up)230.4 kbps

DH+ Station Number	Switch					
	1	2	3	4	5	6
0	on	on	on	on	on	on
1	off	on	on	on	on	on
2	on	off	on	on	on	on
3	off	off	on	on	on	on
4	on	on	off	on	on	on
5	off	on	off	on	on	on
6	on	off	off	on	on	on
7	off	off	off	on	on	on
10	on	on	on	off	on	on
11	off	on	on	off	on	on
12	on	off	on	off	on	on
13	off	off	on	off	on	on
14	on	on	off	off	on	on
15	off	on	off	off	on	on
16	on	off	off	off	on	on
17	off	off	off	off	on	on
20	on	on	on	on	off	on
21	off	on	on	on	off	on
22	on	off	on	on	off	on
23	off	off	on	on	off	on
24	on	on	off	on	off	on
25	off	on	off	on	off	on
26	on	off	off	on	off	on
27	off	off	off	on	off	on
30	on	on	on	off	off	on
31	off	on	on	off	off	on
32	on	off	on	off	off	on
33	off	off	on	off	off	on
34	on	on	off	off	off	on
35	off	on	off	off	off	on
36	on	off	off	off	off	on
37	off	off	off	off	off	on

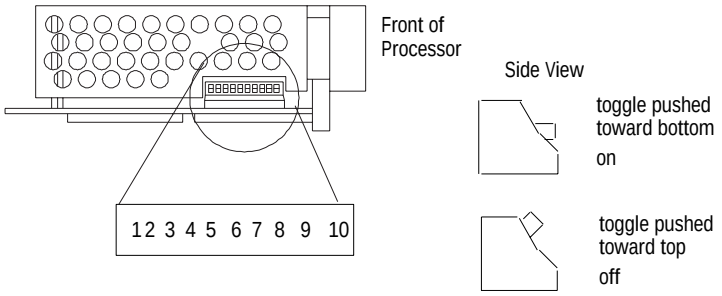
DH+ Station Number	Switch					
	1	2	3	4	5	6
40	on	on	on	on	on	off
41	off	on	on	on	on	off
42	on	off	on	on	on	off
43	off	off	on	on	on	off
44	on	on	off	on	on	off
45	off	on	off	on	on	off
46	on	off	off	on	on	off
47	off	off	off	on	on	off
50	on	on	on	off	on	off
51	off	on	on	off	on	off
52	on	off	on	off	on	off
53	off	off	on	off	on	off
54	on	on	off	off	on	off
55	off	on	off	off	on	off
56	on	off	off	off	on	off
57	off	off	off	off	on	off
60	on	on	on	on	off	off
61	off	on	on	on	off	off
62	on	off	on	on	off	off
63	off	off	on	on	off	off
64	on	on	off	on	off	off
65	off	on	off	on	off	off
66	on	off	off	on	off	off
67	off	off	off	on	off	off
70	on	on	on	off	off	off
71	off	on	on	off	off	off
72	on	off	on	off	off	off
73	off	off	on	off	off	off
74	on	on	off	off	off	off
75	off	on	off	off	off	off
76	on	off	off	off	off	off
77	off	off	off	off	off	off

Switch 2

Bottom View of PLC-5/11, -5/20, -5/26, and -5/20E processors Switch Assembly SW2



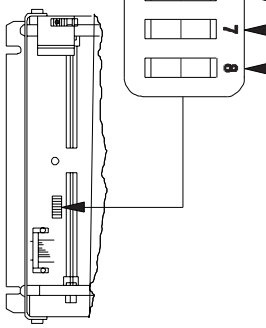
Bottom View of PLC-5/30, -5/40, -5/46 -5/40L, -5/60, -5/60L, -5/80, -5/86, -5/40E, and -5/80E processors Switch Assembly SW2



To Specify:	**Set Switches:**									
	1	2	3	4	5	6	7	8	9	10
RS-232C	on	on	on	off	off	on	on	off	on	off
RS-422A	off	off	on	off	off	off	off	off	on	off
RS-423	on	on	on	off	off	on	off	off	on	off

I/O Chassis Backplane

PLC-5 Controller in the I/O Chassis



Always Off

Switch	Last State
1	
on	Outputs of this I/O chassis remain in their last state when a hardware failure occurs. ①
off	Outputs of this I/O chassis are turned off when a hardware failure occurs. ①

Switches		Addressing
4	5	
off	off	2 - slot
off	on	1 - slot
on	off	1/2 - slot
on	on	Not allowed

Switches		Memory Module Transfer
6	7	
off	off	memory module transfer to processor memory at powerup. ② ③
on	on	memory module transfers to processor memory if processor memory not valid.
on	off	memory module does not transfer to processor memory.

Switch	Processor Memory Protection
8	
off	Processor memory protection disabled.
on	Processor memory protection enabled. ④

Pressed in at top ON (closed)

Pressed in at bottom OFF (open)

① Regardless of this switch setting, outputs are turned off when any of the following occurs:
- processor detects a major fault
- an I/O chassis backplane fault occurs
- you select program or test mode
- you set a status file bit to reset a local rack

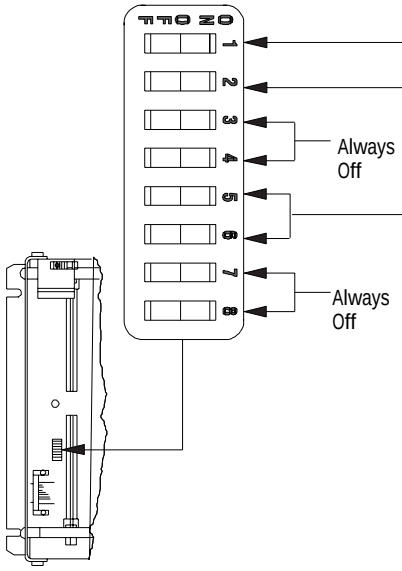
② If a memory module is not installed and processor memory is valid, the processor's PROC LED indicator blinks, and the processor sets S:11/9 in the major fault status word. Power down the processor chassis and either install the correct memory module or set switch 6 ON.

③ If the processor's keyswitch is set in REMote, the processor enters remote RUN after it powers up and has its memory updated by the memory module.

④ You cannot clear processor memory when this switch is on.

19309

1771-ASB Remote I/O Adapter or 1771-ALX Extended-Local I/O Adapter



Switch 1	Last State
on	Outputs of this I/O chassis remain in their last state when a communication fault is detected by this I/O adapter. ①
off	Outputs of this I/O chassis are turned off when a communication fault is detected by this I/O adapter.

Switch 2	Processor Restart Lockout
on	Processor can restart the I/O chassis after a communication fault. ②
off	You must manually restart the I/O chassis with a switch wired to the 1771-AS or -ASB.

Switches 5	Switches 6	Addressing
off	off	2-slot
on	off	1-slot ③
off	on	1/2-slot ③
on	on	Not allowed

Pressed in at top ON (closed)

Pressed in at bottom OFF (open)

19308

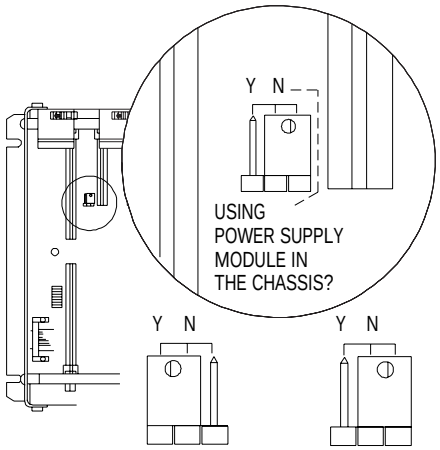
ATTENTION

If you set this switch to the ON position, when a communication fault is detected, outputs connected to this chassis remain in their last state to allow machine motion to continue. We recommend that you set switch 1 to the OFF position to de-energize outputs wired to this chassis when a fault is detected.

Also, if outputs are controlled by inputs in a different rack and a remote I/O rack fault occurs (in the inputs rack), the inputs are left in their last non-faulted state. The outputs may not be properly controlled and potential personnel and machine damage may result. If you want your inputs to be anything other than their last non-faulted state, then you need to program a fault routine.

Set this switch to ON if you plan to use I/O rack auto-configuration. The 1771-ASB series A adapter does not support 1/2-slot addressing.

I/O Chassis Configuration Plug



Set Y when you install a power supply module in the chassis.

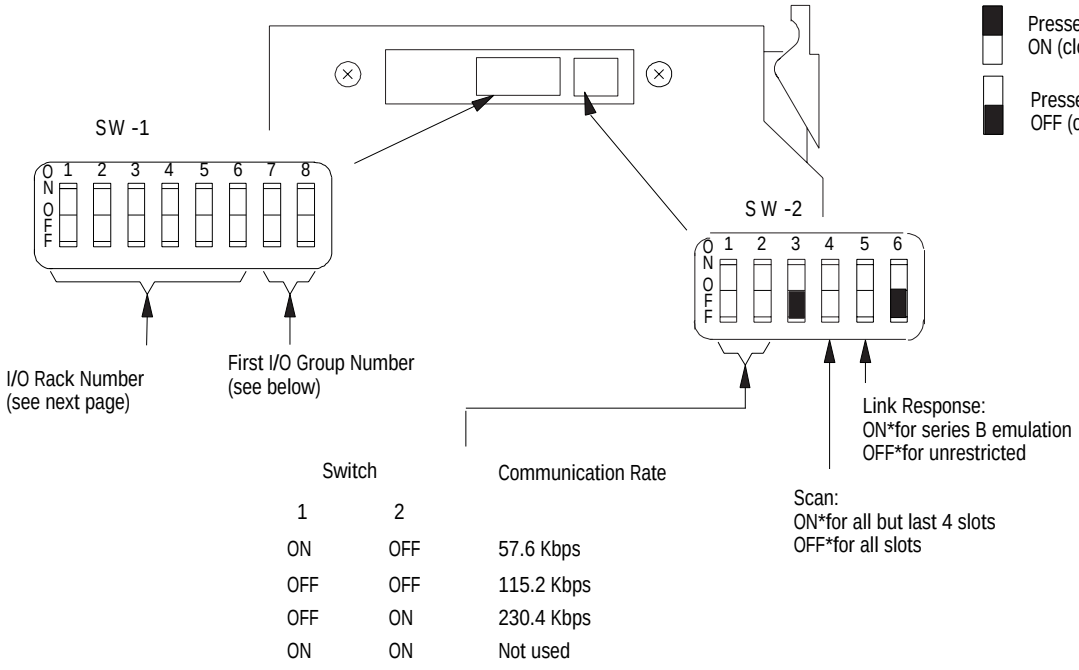
Set N when you use an external power supply.

1. Locate the chassis configuration plug (between the first two left-most slots of the chassis).
2. Set the I/O chassis configuration plug. The default setting is N (not using a power supply module in the chassis).

Important: You cannot power a single I/O chassis with both a power supply module and an external power supply.

17075

Remote I/O Adapter Module (1771-ASB Series C and D) without Complementary I/O



Switch 1	Switch 2	Communication Rate
ON	OFF	57.6 Kbps
OFF	OFF	115.2 Kbps
OFF	ON	230.4 Kbps
ON	ON	Not used

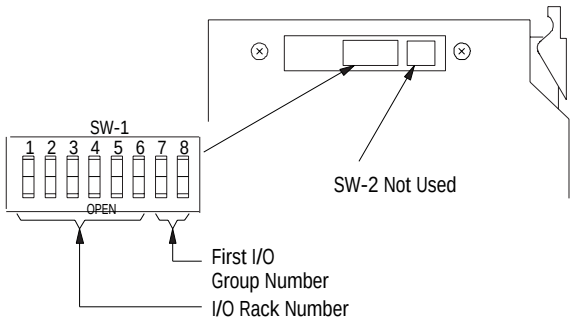
First I/O Group Number:	**7**	**8**
0	on	on
2	on	off
4	off	on
6	off	off

(1771-ASB Series C and D) I/O Rack Number - without Complementary I/O

Rack	1	2	3	4	5	6
01	on	on	on	on	on	off
02	on	on	on	on	off	on
03	on	on	on	on	off	off
04	on	on	on	off	on	on
05	on	on	on	off	on	off
06	on	on	on	off	off	on
07	on	on	on	off	off	off
10	on	on	off	on	on	on
11	on	on	off	on	on	off
12	on	on	off	on	off	on
13	on	on	off	on	off	off
14	on	on	off	off	on	on
15	on	on	off	off	on	off
16	on	on	off	off	off	on
17	on	on	off	off	off	off
20	on	off	on	on	on	on
21	on	off	on	on	on	off
22	on	off	on	on	off	on
23	on	off	on	on	off	off
24	on	off	on	off	on	on
25	on	off	on	off	on	off
26	on	off	on	off	off	on
27	on	off	on	off	off	off

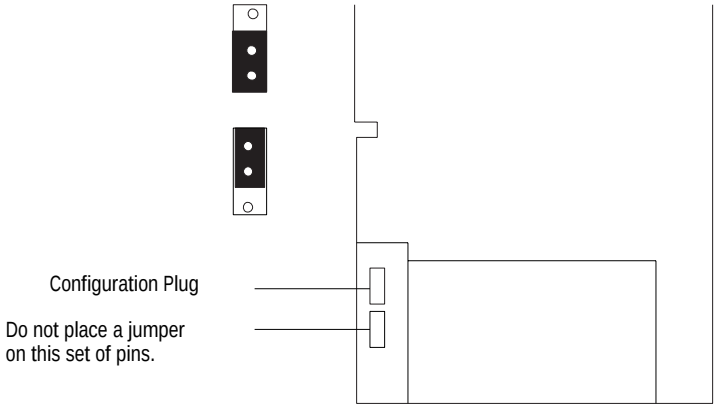
Extended-Local I/O Adapter Module

(1771-ALX) Switch SW1



Rack:	1	2	3	4	5	6
01	on	on	on	on	on	off
02	on	on	on	on	off	on
03	on	on	on	on	off	off
04	on	on	on	off	on	on
05	on	on	on	off	on	off
06	on	on	on	off	off	on
07	on	on	on	off	off	off
10	on	on	off	on	on	on
11	on	on	off	on	on	off
12	on	on	off	on	off	on
13	on	on	off	on	off	off
14	on	on	off	off	on	on
15	on	on	off	off	on	off
16	on	on	off	off	off	on
17	on	on	off	off	off	off
20	on	off	on	on	on	on
21	on	off	on	on	on	off
22	on	off	on	on	off	on
23	on	off	on	on	off	off
24	on	off	on	off	on	on
25	on	off	on	off	on	off
26	on	off	on	off	off	on
27	on	off	on	off	off	off

(1771-ALX) Configuration Plug



1. Lay the module on its right side.

   The configuration plugs are visible on the lower rear of the module.

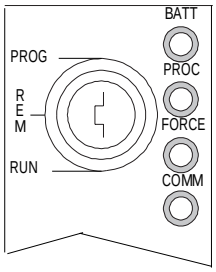
2. Set the configuration plug as shown below according to your application.

If You are Using	But Not	Set Configuration Plug
32-point I/O modules and any address method	1771-IX or 1771-IY	on the 2 lower pins
1771-IX and 1771-IY modules and any addressing method	32-point I/O modules	on the 2 upper pins

Troubleshooting

Using This Chapter

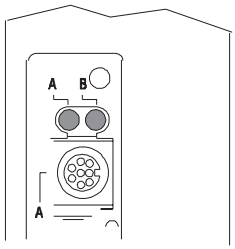
PLC-5 Controller General Problems



Indicator	Color	Description	Probable Cause	Recommended Action
PROC	Green (steady)	Controller is in run mode and fully operational	Normal operation	No action required
	Green (blinking)	Controller memory is being transferred to EEPROM	Normal operation	No action required
	Red (blinking)	Major fault	• RSLogix 5 download in progress • Run-time error	During RSLogix 5 download, this is normal operation - wait for download to complete. If not during RSLogix 5 download: • Check major fault bit in status file (S:11) for error definition • Clear fault, correct problem, and return to run mode
	Alternating Red and Green	Controller in FLASH-memory programming mode	Normal operation if controller's FLASH memory is being reprogrammed	No action required - allow flash update to complete
	Red (steady)	Power cycle with problem battery	Battery is low, disconnected or not installed	Properly replace or install battery (see Chapter 1 for more information)
	Red (steady)	Fault with memory loss	New controller Invalid ControlNet network address Controller has failed internal diagnostics	Use programming software to clear and initialize memory Verify that ControlNet address switch is not set to 0 Install battery (to preserve failure diagnostics), then power down, reseat controller and power up; then reload your program. If you are unable to reload your program, replace the controller. If you are able to reload your program and fault persists, contact Technical Support at 440.646.6800 to diagnose the problem.
	Off	Controller is in program load or test mode or is not receiving power		Check power supply and connections

Indicator	Color	Description	Probable Cause	Recommended Action
FORCE	Amber (steady)	SFC and/or I/O forces enabled	Normal operation	No action required
	Amber (blinking)	SFC and/or I/O forces present but not enabled		
	Off	SFC and/or I/O forces not present		
COMM	Off	No transmission on channel 0	Normal operation if channel is not being used	
	Green (blinking)	Transmission on channel 0	Normal operation if channel is being used	

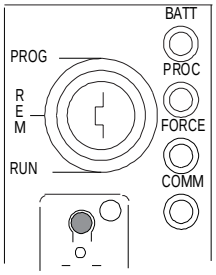
Controller Communication Channel Troubleshooting



Indicator	Color	Channel Mode	Description	Probable Cause	Recommended Action
A or B	Green (steady)	Remote I/O Scanner	Active Remote I/O link, all adapter modules are present and not faulted	Normal operation	No action required
		Remote I/O Adapter	Communicating with scanner		
		DH+	Controller is transmitting or receiving on DH+ link		
	Green (blinking rapidly or slowly)	Remote I/O Scanner	At least one adapter is faulted or has failed	• Power off at remote rack • Cable broken	• Restore power to the rack • Repair cable
		DH+	No other nodes on network		
	Red (steady)	Remote I/O Scanner Remote I/O Adapter DH+	Hardware fault	Hardware error	Turn power off, then on Check that the software configurations match the hardware set-up Replace the controller.
	Red (blinking rapidly or slowly)	Remote I/O Scanner	All adapters faulted	• Cable not connected or broken • Power off at remote racks	• Repair cable • Restore power to racks
		DH+	Bad communication on DH+	Duplicate node detected	Correct station address
	Off	Remote I/O Scanner Remote I/O Adapter DH+	Channel offline	Channel is not being used	Place channel online if needed

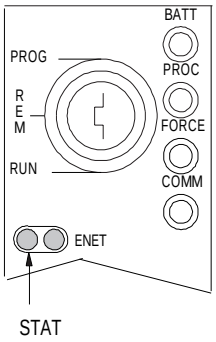
Extended-Local I/O Troubleshooting

PLC-5/40L and -5/60L processors only

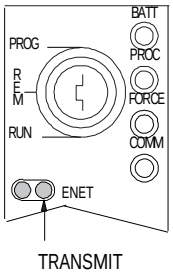


Indicator	Color	Channel Mode	Description	Probable Cause	Recommended Action
2	green (steady)	Extended local I/O Scanner	active extended-local I/O link, all adapter modules are present and not faulted	normal operation	no action required
	green (blinking rapidly or slowly)		at least one adapter is faulted or has failed	• power off at extended-local I/O rack • communication fault • cable broken	• restore power to the rack • restart adapters using the controller restart lockout pushbutton • repair cable
	red (steady)		hardware fault	hardware error	Turn power off, then on. Check that the software configurations match the hardware set-up. Replace the controller.
	red (blinking rapidly or slowly)	Extended local I/O Scanner	all adapters faulted	• cable disconnected or broken • terminator off • power off at extended-local racks	• repair cable • replace or repair terminator • restore power to racks
	off		channel offline	channel is not being used	Place channel online if needed

Ethernet Status Indicator



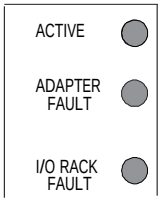
Indicator	Color	Description	Probable Cause	Recommended Action
STAT	Solid red	Critical hardware fault	Controller requires internal repair	Contact your local Allen-Bradley representative
	Blinking red	Hardware or software fault (detected and reported via a code)	Fault-code dependent	Contact Allen-Bradley's Global Technical Support (GTS)
	Off	Ethernet interface is functioning properly but it is not attached to an active Ethernet network	Normal operation	Attach the Controller to an active Ethernet network
	Green	Ethernet channel 2 is functioning properly and has detected that it is connected to an active Ethernet network	Normal operation	No action required



Ethernet Transmit LED

The PLC-5 Ethernet interface contains an Ethernet Transmit LED that lights (green) briefly when the Ethernet port is transmitting a packet. It does not indicate whether or not the Ethernet port is receiving a packet.

Remote I/O System



Troubleshooting Guide for the 1771-ASB Series C and D Adapter Module

Indicators			Description	Probable Cause	Recommended Action
Active	Adapter Fault	I/O Rack			
On	Off	Off	Normal indication; remote adapter is fully operational		
Off	On	Off		RAM memory fault, watchdog timeout	Replace module.
On	Blink	Off	Module placement error	I/O module in incorrect slot.	Place module in correct slot in chassis.
Blink in unison		Off	Incorrect starting I/O group number	Error in starting I/O group number or I/O rack address	Check switch settings.
On	On	On	Module not communicating	Incorrect transmission rate setting	
Off	On	On	Module not communicating	Scan switch set for “all but last four slots” in 1/4 rack	Reset scan switch setting.
Blink	Off	Off	Remote adapter not actively controlling I/O (scanner to adapter communication link is normal)(1)	Controller is in program or test mode Scanner is holding adapter module in fault mode	Fault should be cleared by I/O scanner.
LEDs sequence on/off from top to bottom			Module not communicating	Another remote I/O adapter with the same address is on the link.	Correct the address.

Indicators			Description	Probable Cause	Recommended Action
Active	**Adapter Fault**	**I/O Rack**			
Blink alternately		Off	Adapter module not actively controlling I/O[2] Adapter module in controller restart lockout mode (adapter to scanner link is normal)	Controller restart lockout switch on chassis backplane switch assembly on[3]	Press reset button to clear lockout feature or cycle power; if after repeated attempts indicators are still blinking, check: • push button not wired properly to field wiring arm • wiring arm not connected to adapter module • adapter module was reset by process or/ scanner, then immediately faulted

(1) If a fault occurs and the Controller is in the run mode but is actually operating in the dependent mode, the chassis fault response mode is selected by the last state switch on the chassis backplane.

(2) The I/O chassis is in faulted mode as selected by the last state switch on the chassis backplane.

(3) You must select the operating mode of the remote I/O adapter module as outlined in the publication furnished with the remote I/O scanner/distribution panel, remote I/O scanner-program interface module, or I/O scanner-message handling module. Pay close attention to the disable search mode in the 1771-SD, -SD2.

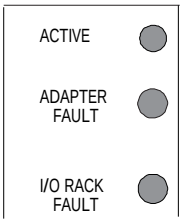
Troubleshooting Guide for the 1771-ASB Series C and D Adapter Module (continued)

Indicators			Description	Probable Cause	Recommended Action
Active	**Adapter Fault**	**I/O Rack**			
Off	Off	On	I/O chassis fault. (1) No communication on link.	Problem exists between: • adapter and module in chassis; the module will stay in fault mode until fault is corrected • shorted printed circuit board runs on backplane or I/O module	Cycle power to the chassis to clear a problem resulting from high noise.(2) • Remove and replace all I/O modules one at a time • If problem does not clear, something is wrong in chassis or I/O module
Blink	Off	On	Communication on link. Possible shorted backplane	• Noise on backplane • Shorted circuit board runs • Faulty card in chassis	• Eliminate noise • Isolate noise • Add surge suppression • Replace chassis • Replace defective card in chassis
Blink	On	Off	Module identification line fault	Excessive noise on backplane	Verify power supply and chassis grounding.
Off	Off	Off	Module not communicating	Power supply fault	Check power supply, cable connections, and make sure adapter module is fully seated in chassis.
				Wiring from scanner to adapter module disrupted	Correct cable and wiring defects
				Scanner not configured properly	See publication 1772-2.18 for scanner configuration.
				One faulted chassis within a rack group address causing scanner/distribution panel to fault all chassis in rack group address (when in disable search mode)	Check sequentially from the first module to the last module to pinpoint fault; correct any faults and proceed to the next chassis.

(1) The I/O chassis is in faulted mode as selected by the last state switch on the chassis backplane.

(2) Cycling power clears block-transfer request queue. All pending block transfers are lost. Your program must repeat the request for block transfers.

Extended-Local I/O System Troubleshooting Guide for the 1771-ALX Adapter Module



Indicators			Description	Probable Cause	Recommended Action
Active	**Adapter Fault**	**I/O Rack**			
On	Off	Off	Normal indication; remote adapter is fully operational		
Off	On	Off	Local adapter fault (1)	Local adapter not operating; it will stay in fault mode until fault is corrected	Cycle power to the chassis to clear the adapter fault.(2) Replace adapter if fault does not clear.
Off	Off	On	I/O chassis fault 1	Problem exists between: • adapter and module in chassis; the module will stay in fault mode until fault is corrected • shorted printed circuit board runs on backplane or I/O module	Cycle power to the chassis to clear a problem resulting from high noise.2 • remove and replace all I/O modules one at a time • replace adapter • If problem does not clear, something is wrong in chassis or I/O module
Blinking	Off	Off	Outputs are reset	Controller is in program or test mode Local I/O Scanner is holding adapter module in fault mode	None Fault should be cleared by extended-local I/O scanner.
Blinking alternately		Off	Adapter module not actively controlling I/O 1 Adapter module in controller restart lockout mode (adapter to scanner link is normal)	Controller restart lockout switch on chassis backplane switch assembly on(3)	Press chassis reset button to clear lockout feature or cycle power; if after repeated attempts indicators are still blinking, check that adapter module was reset by controller/scanner, then immediately faulted.
Off	Off	Off	No power or no communication.	Power supply fault	Check power supply, I/O cable and power supply cable connections, and make sure adapter module is fully seated in chassis.
On	Blinking	Off	Module placement error in extended-local I/O chassis	Incorrect placement of high-density modules	Verify addressing modes and switch settings.

(1) Cycling power clears the block-transfer request queue. All pending block transfers are lost. Your program must repeat the request for block transfers from the chassis.

(2) If a fault occurs and the controller is in the run mode but is actually operating in the dependent mode, the chassis fault response mode is selected by switch 1 (the last state switch) on the chassis backplane.

(3) The I/O chassis is in faulted mode as selected by switch 1 (the last stare switch) on the chassis backplane.

Unexpected Operation when Entering Run Mode

If unexpected operation occurs whenever your controller enters run mode, be sure to examine the prescan operation of the instructions in this section. These instructions execute differently during prescan than they do during a normal scan.

The prescan function is an intermediate scan between the transition from program to run modes, during which all rungs are scanned as false. The prescan examines all ladder program files and instructions and initializes the data table based on the results of the program.

For example, a subroutine that is called infrequently may contain a bad indirect address and generate a major fault. However, many normal program scans may occur before the major fault is actually generated. Prescan provides the opportunity for the controller to examine the program for errors such as this before transitioning to Run mode.

Instructions with Unique Prescan Operations

Use the table below to track prescan operations that deviate from normal instruction operation.

This Instruction:	Executes These Actions During Prescan:
ARD	If the EN bit is set and the DN and ER bits are cleared, then the control word is cleared. If either the DN or ER bit is set, then the EN bit is cleared and the DN bit is set.
ARL	
AWT	
AWA	
ACB	
ABL	
AHL	
BTR	All non-user configuration bits 15, 14, 13, 12, 10, and 9 are cleared (for both INT and BT file types).
BTW	
CTU	The CU/CD bit is set to prevent a false count when the first run-mode scan begins.
CTD	
EOT	This instruction is skipped so all ladder instructions can be prescanned.
FFL	The EL bit is set to prevent a false load when the first run-mode scan begins.
LFL	
FFU	The EU bit is set to prevent a false unload when the first run-mode scan begins.
LFU	
FND	This instruction is skipped so all ladder instructions can be prescanned.

This Instruction:	Executes These Actions During Prescan:
FOR	Ladder instructions within the FOR/NXT loop **are** prescanned.
MSG	If the SFC startover bit is cleared and the CO bit is cleared, then all non-user configuration bits 15, 14, 13, 12, 10, and 9 are cleared in both the INT and MG file types. The MG file type also clears bits 11, 7, 6, 5, 4, 2, 1, and 0.
ONS	The programmed bit address of the instruction is set to inhibit false triggering when the first run-mode scan begins.
OSF	The programmed bit address of the instruction is cleared to inhibit false triggering when the first run-mode scan begins. The output bit is also cleared.
OSR	
PID	For PD file type, the INI bit is cleared. INT file type clears status bits 8, 9, and 10 (deadband, upper, and lower output alarm). The error register from the previous scan is set to 32767, which indicates that the setpoint and ER bits from previous scans have not yet been initialized). The Integral Accumulator and Derivative Error bits are cleared.
SQL	The EN bit is set to prevent a false increment of the table pointer when the first run-mode scan occurs.
SQO	
TOF	The TT, TC, TE, and TO bits are cleared and the ACC = preset.
DTR [1]	The reference value is updated (regardless of the rung condition).

[1] The DTR instruction operates in this manner during a normal scan as well.

Suggested Action

To avoid unexpected operation that may result from these prescan activities, follow these guidelines:

- Do not use indexed or indirect addressing with the instructions listed in the above table.
- If you *must* use indexed or indirect addressing, use the first scan bit (S:1/15) to pre-initialize all of the other used variables.
- If using indirect addressing with any ladder instructions, do not use the data variable holding the indirect address for multiple functions.

Notes

Cable Reference

Using This Chapter

Channel 0 Pin Assignments

The side label of the controller shows a table listing channel 0 (RS-port) pin assignments. This table shows the same information:

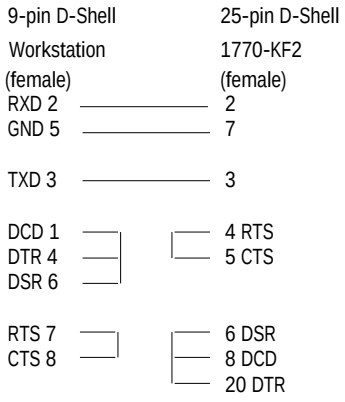
Pin	RS-232C	RS-422A	RS-423	Pin	RS-232C	RS-422A	RS-423
1	C.GND	C.GND	C.GND	14	NOT USED	$TXD.OUT^-$	SEND COM
2	TXD.OUT	$TXD.OUT^+$	TXD.OUT	15			
3	RXD.IN	$RXD.IN^+$	RXD.IN	16	NOT USED	$RXD.IN^-$	REC COM
4	RTS.OUT	$RTS.OUT^+$	RTS.OUT	17			
5	CTS.IN	$CTS.IN^+$	CTS.IN	18			
6	DSR.IN	$DSR.IN^+$	DSR.IN	19	NOT USED	$RTS.OUT^-$	NOT USED
7	SIG.GND	SIG.GND	SIG.GND	20	DTR.OUT	$DTR.OUT^+$	DTR.OUT
8	DCD.IN	$DCD.IN^+$	DCD.IN	21			
9				22	NOT USED	$DSR.IN^-$	NOT USED
10	NOT USED	$DCD.IN^-$	NOT USED	23	NOT USED	$DTR.OUT^-$	NOT USED
11				24			
12				25			
13	NOT USED	$CTS.IN^-$	NOT USED				

The shading indicates that the pin is reserved.

Serial Cable Pin Assignments

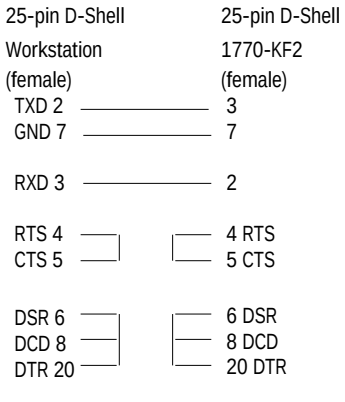
The following diagrams show the pin assignments for the cables you need for serial port communications.

Cable #1



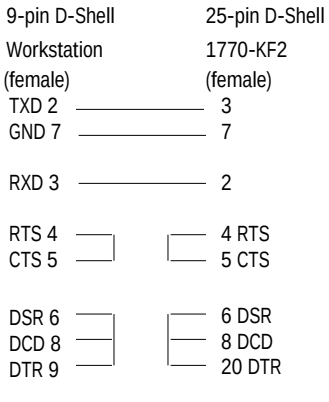
11955-I

Cable #2



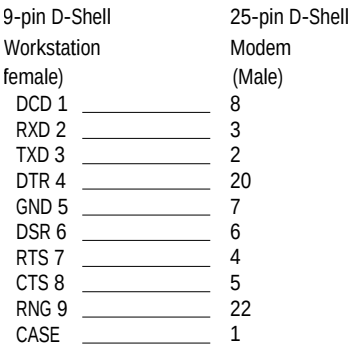
11957-I

Cable #3



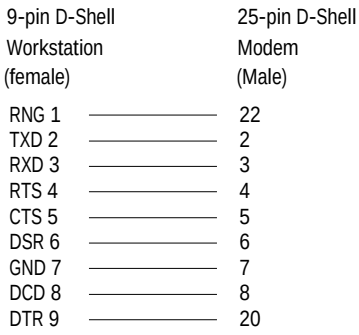
11958-I

Cable #4



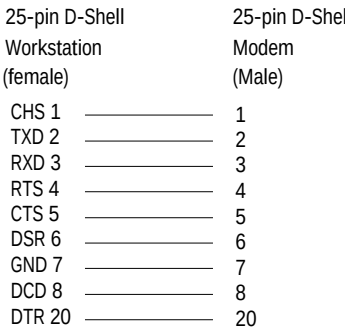
11959-I

Cable #5



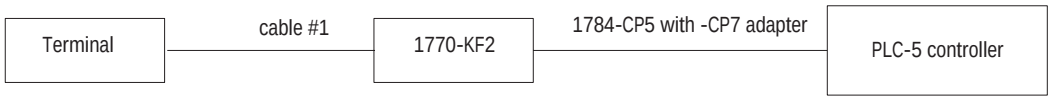
11960-I

Cable #6



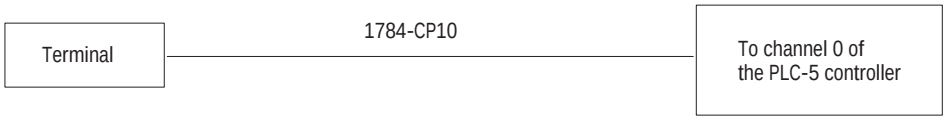
11961-I

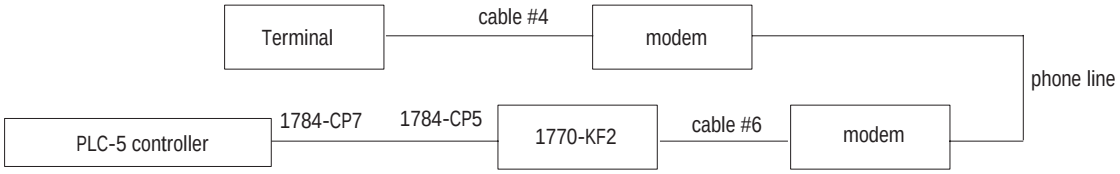
Connecting Diagrams

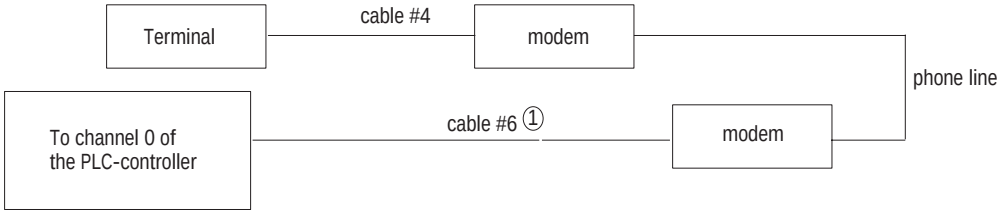


9-Pin Serial Port Workstation

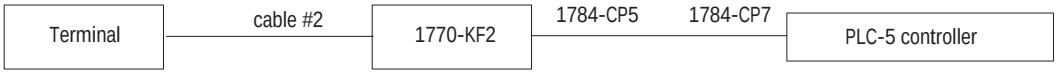
Note: 1785-KE Series A uses 1785-CP5 cable and 1785-CP7 adapter with the Enhanced and Ethernet PLC-5 Programmable Controllers





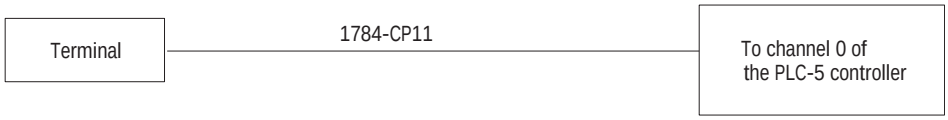


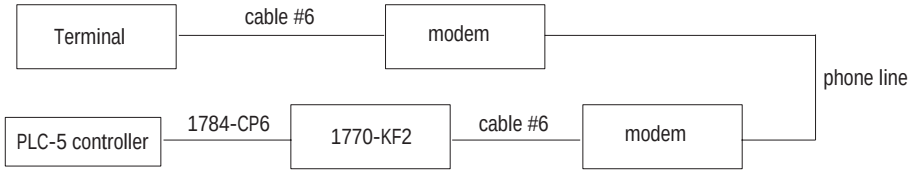
① Requires either a gender changer or one end of cable #2 fitted with a male 25-pin plug.

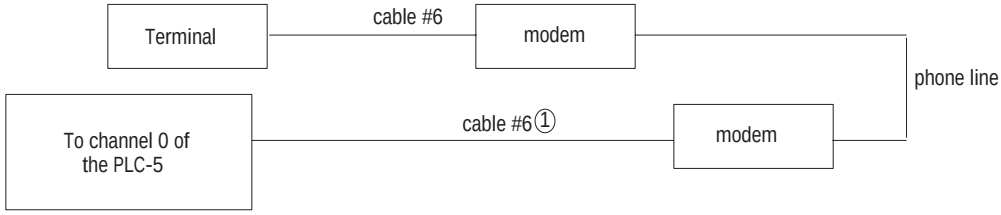


25-Pin Serial Port Workstation

Note: 1785-KE Series A uses 1785-CP5 cable and 1785-CP7 adapter with the Enhanced and Ethernet PLC-5 controller







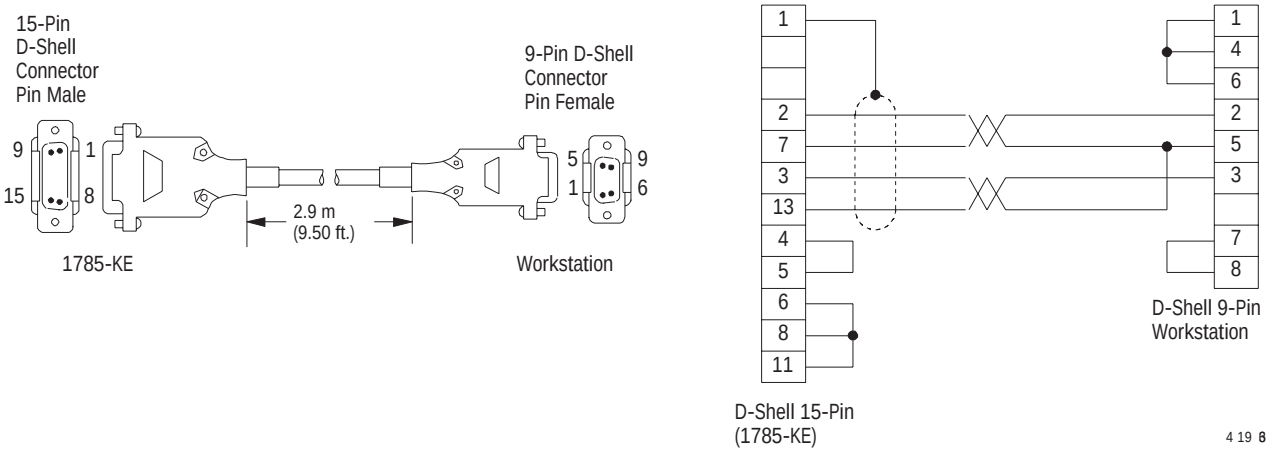
① Requires either a gender changer or one end of cable #2 fitted with a male 25-pin plug.

Programming Cable Specifications

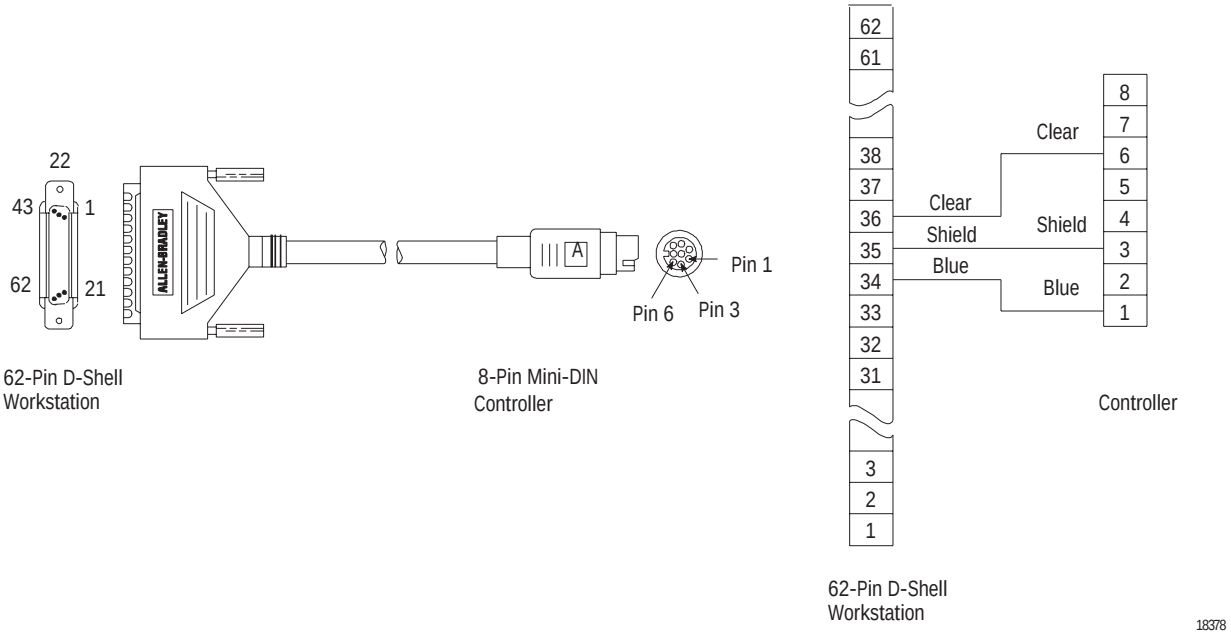
The specifications for each Allen-Bradley cable used for DH+ communications are shown on the following pages. Refer to the following table for the exact location.

For	To	Use this Cable	See Page
Workstation	1785-KE	1784-CAK	25-5
Enhanced or Ethernet PLC-5 controller	Workstation (using a 1784-KT, -KT2, -KL, or -KL/B)	1784-CP6 1784-CP with a 1784-CP7 adapter 1784-CP8 adapter	25-6 25-6 25-7
	Workstation (using a 1784-KTK1)	1784-CP5 with a 1785-CP7 adapter	25-6
	Workstation (using a 9-pin serial cable)	1784-CP10	25-7
	Workstation (using a serial 25-pin cable)	1784-CP11	25-8
	Workstation (using a 1784-PCMK)	1784-PCM5 with a 1784-CP7 adapter	25-8 and 25-6

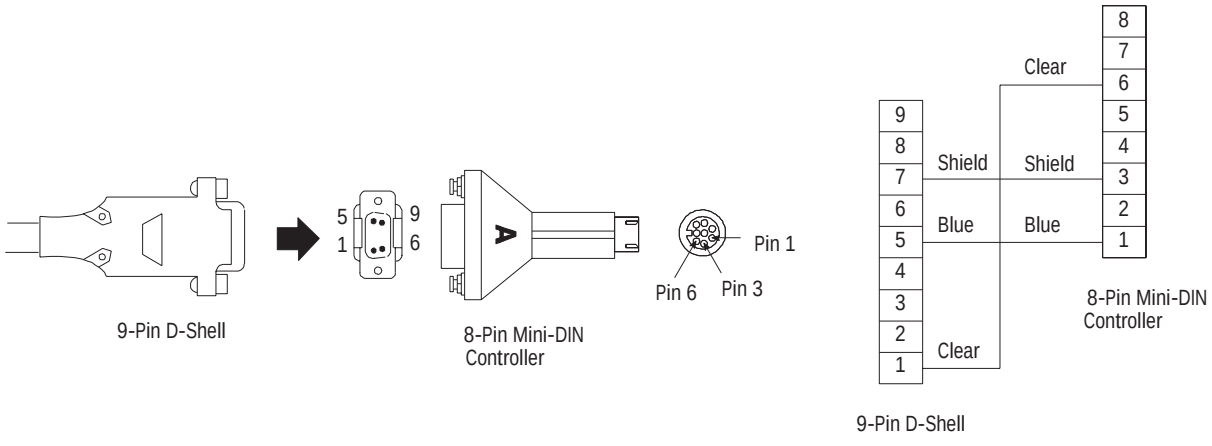
Cable - 1784-CAK
Connects 1785-KE to WorkstationT



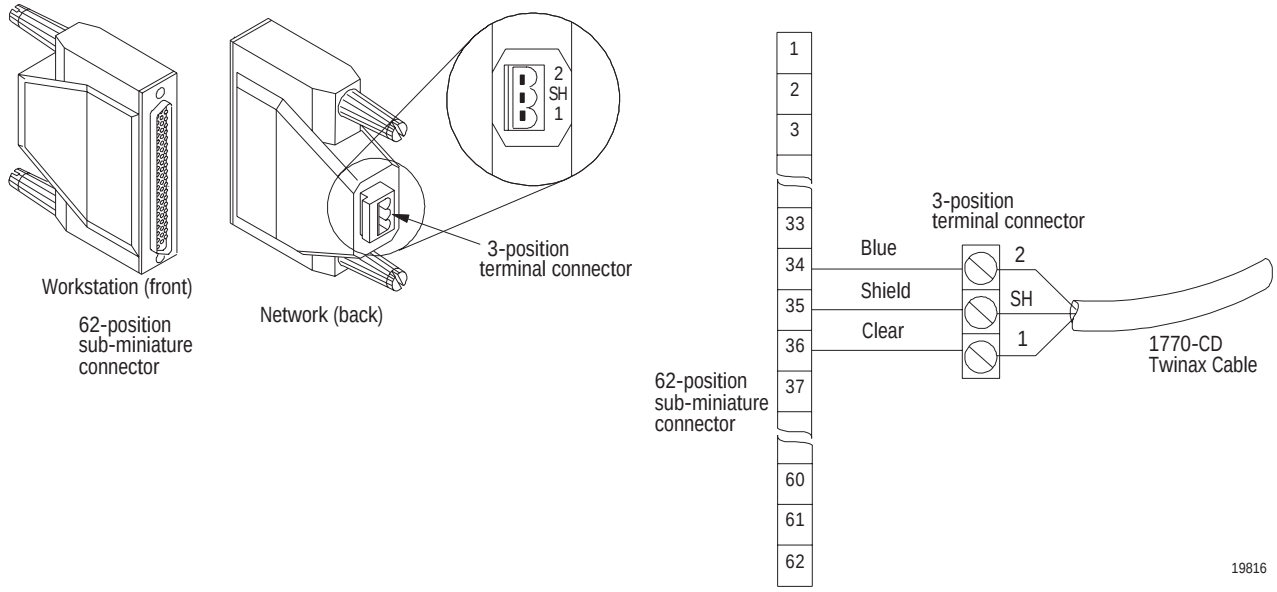
Cable - 1784-CP6
Connects Workstation Using 1784-KT, -KT/2, -KL, or -KL/B to Controller



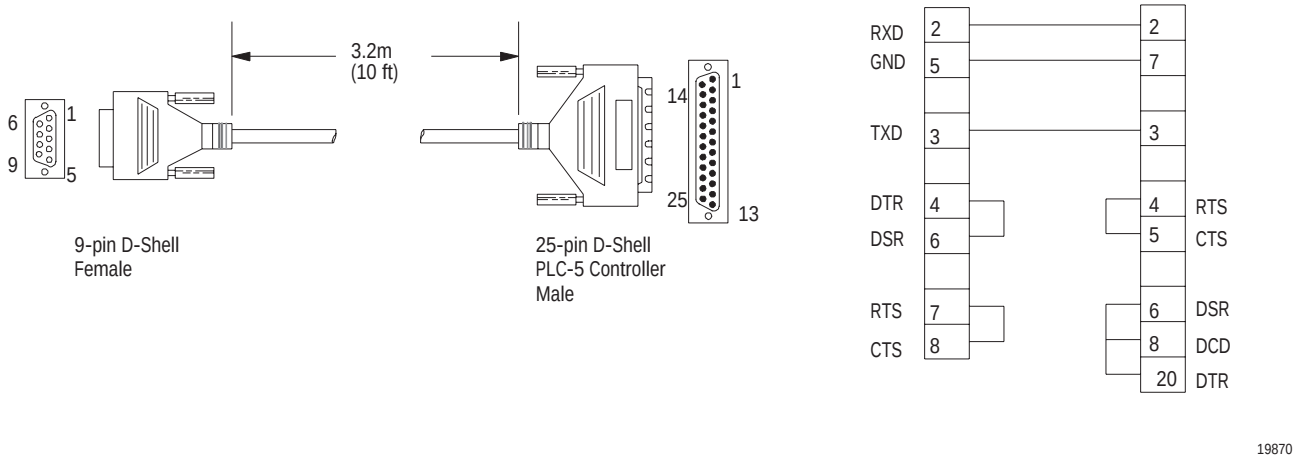
Cable and Adapter - 1784-CP7 Connects to Controller via 9-pin D-Shell of a 1784-CP, -CP5, or -PCM5 cable



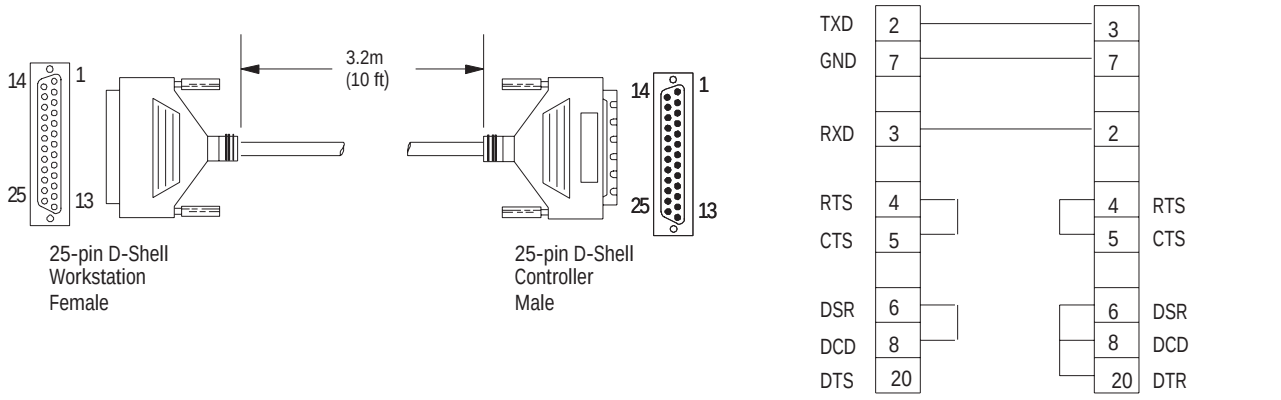
Cable Adapter - 1784-CP8 Connects a Workstation Using a 1784-KT, -KT2, or -KL Card to a Permanent DH+ Network



Cable - 1784-CP10
Connects Workstation to Controller Using Serial Port



Cable - 1784-CP11
Controller to Workstation Using a Serial Port



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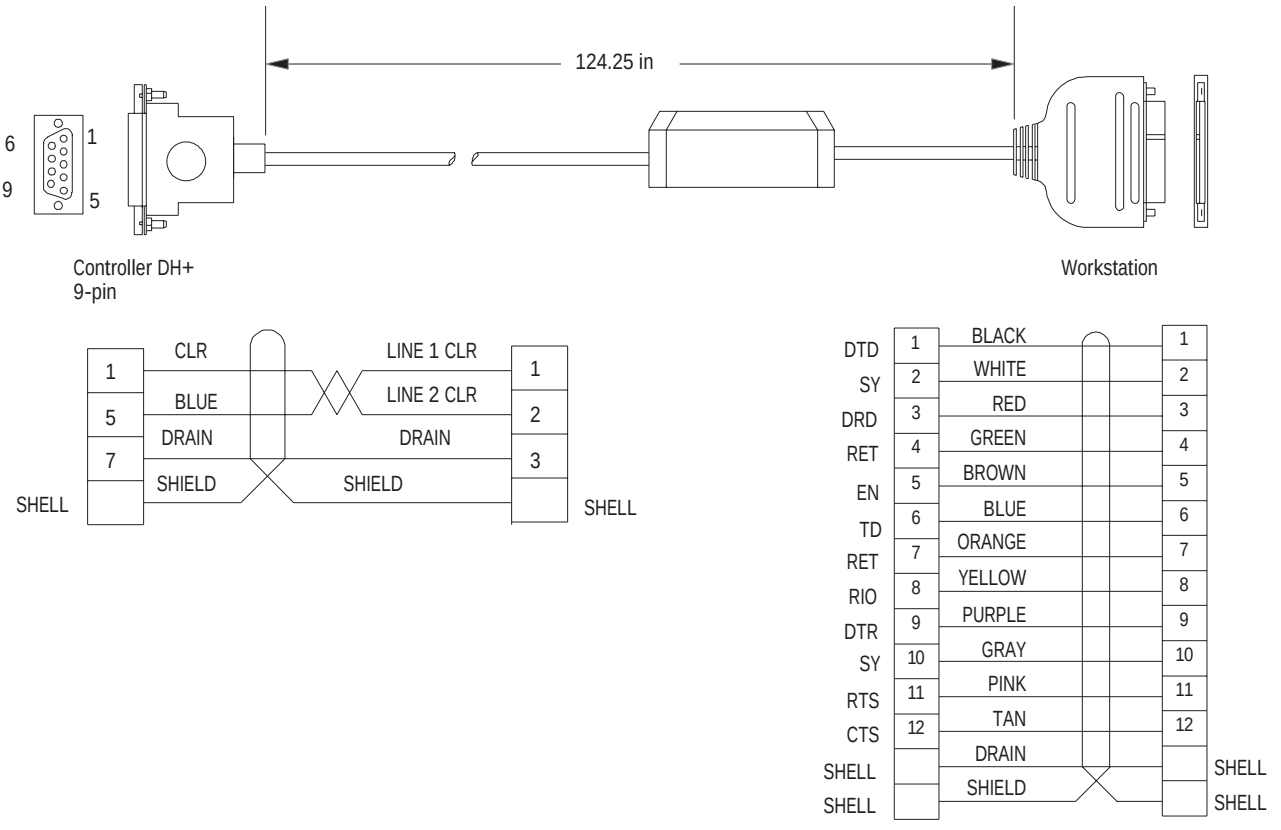
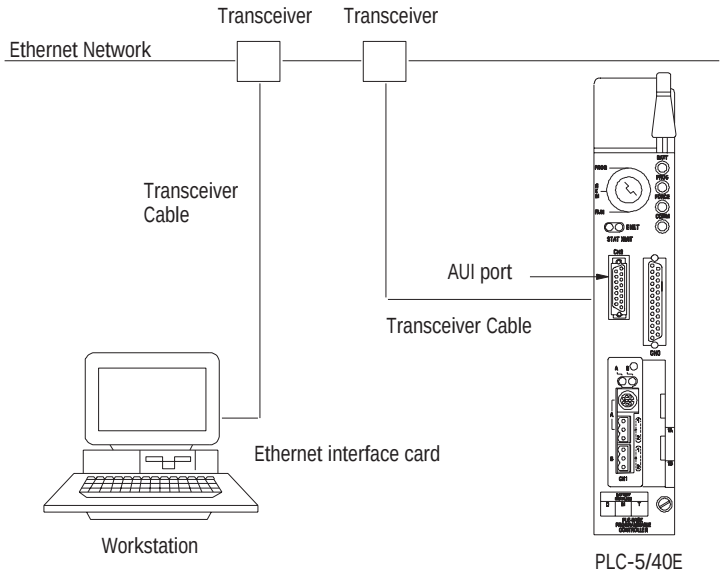
Cable - 1784-PCM5
Controller to Workstation (using a 1784-PCMK)



19872

Ethernet Cable Connections

The Ethernet port connects to either a thin-wire or thick-wire network via a 15-pin transceiver or Medium Access Unit (MAU) connection.



To connect a programming terminal to a PLC-5/20E, -5/40E, or -5/80E controller through an Ethernet network, use the following:

- Ethernet PCMCIA or PC/AT-compatible (6628-A5) communication card
- Ethernet cable
- Transceivers and transceiver cables

The table below describes Allen-Bradley transceivers:

Catalog Number	Description
1785-TR10BT	Twisted pair transceiver
1785-TR10BF	Optical transceiver
1785-TR10B2	Thin-wire transceiver
1785-TR10B5	Thick-wire transceiver
5810-AXMT	Thin-wire Ethernet/802.3 transceiver
5810-AXMH	Thick-wire Ethernet/802.3 transceiver

The controller connects to the transceiver using a standard transceiver cable, which is also known as an Access Unit Interface (AUI) cable. Allen-Bradley has two lengths of transceiver cables and four kits consisting of transceivers and cables.

Catalog Number	Description
5810-TER	Thinwire Ethernet terminating resistors
5810-TC02/A	Thick-wire 2.0 m (6.5 ft) transceiver cable
5810-TC15/A	Thick-wire 15.0 m (49.2 ft) transceiver cable
5810-TAS/A (kit)	Thin-wire transceiver and 2.0 m (6.5 ft) cable
5810-TAM/A (kit)	Thin-wire transceiver and 15.0 m (49.2 ft) cable
5810-TBS/A (kit)	Thick-wire transceiver and 2.0 m (6.5 ft) cable
5810-TBM/A (kit)	Thick-wire transceiver and 15.0 m (49.2 ft) cable

Connection to “10baseT” (fiber-optic) and broadband networks is also supported if you purchase the appropriate transceivers and cables from a third-party source.

Numerics

A

B

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D

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F

R

S

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U

W

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